高纯锗CMOS-ASIC电子学研究进展

邓智 何力 刘丰 郝嘉俊 叶祥珂
清华大学-工程物理系

2023-5-9

第二届地下和空间粒子物理与宇宙物理前沿问题研讨会
国科大杭高院基地 ● 2023年5月7日-12日

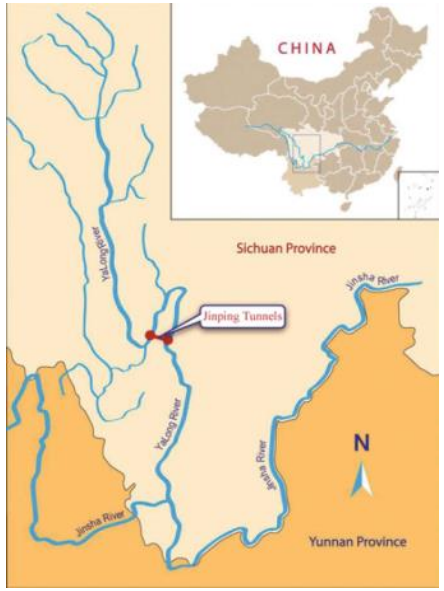
CJPL

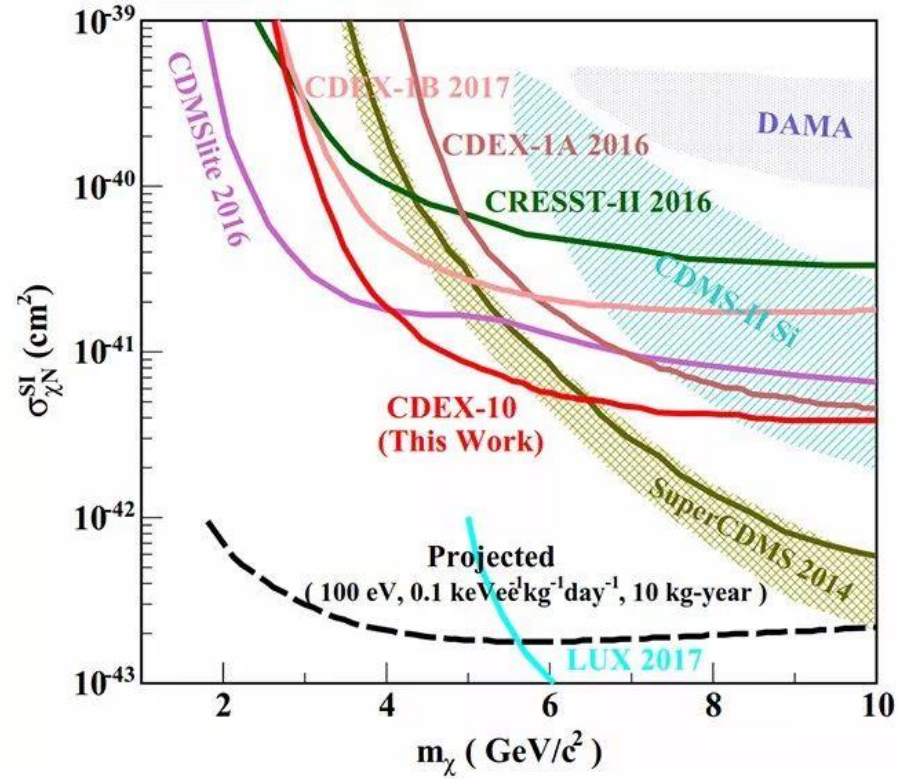
概要

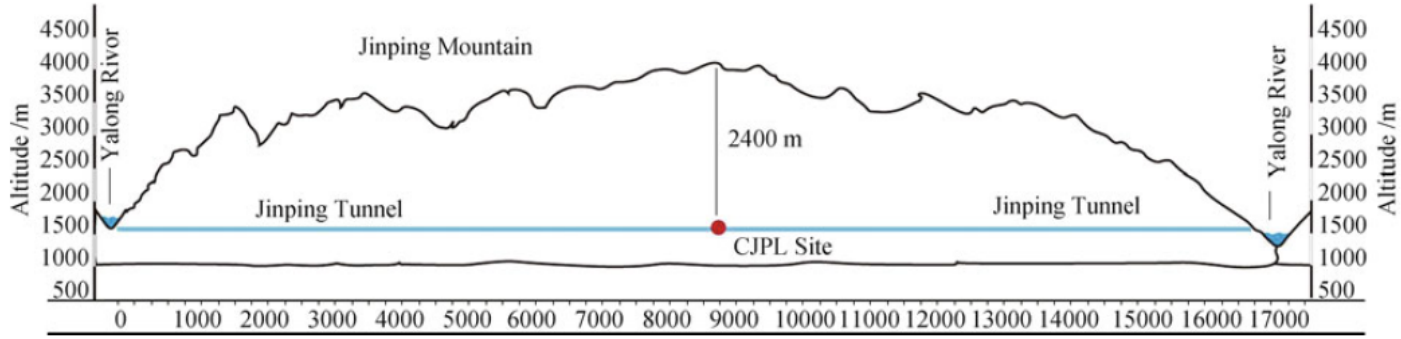
- 背景
- 研究进展：
  - 低温MOS晶体管模型
  - 低温低噪声、宽动态CMOS前放ASIC
  - 低温SCA波形采样ASIC
- 小结

背景

- CDEX实验
  - 在锦屏地下实验室开展的基于高纯锗探测器的直接暗物质探测实验
  - CDEX1→CDEX10→CDEX100/200



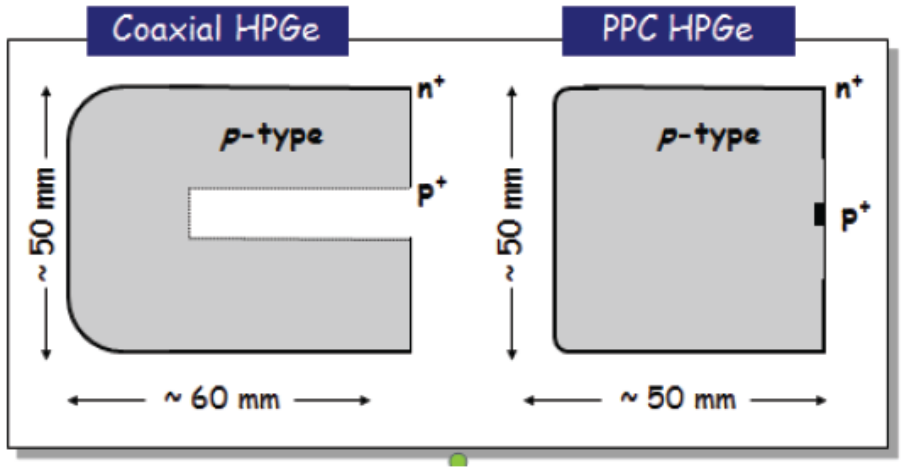


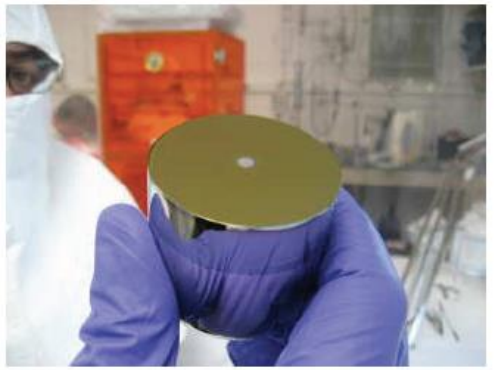


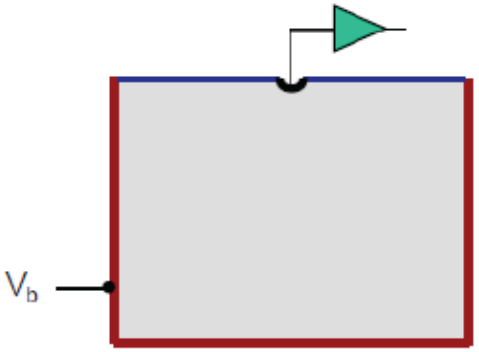
CJPL

点电极高纯锗探测器

- 采用点电极收集电荷，可实现大体积、小电容，从而降低暗物质探测阈值
- 暗物质和0vbb探测实验：
  - Cogent, CDEX
  - GERDA, MAJORANA, LEGEND





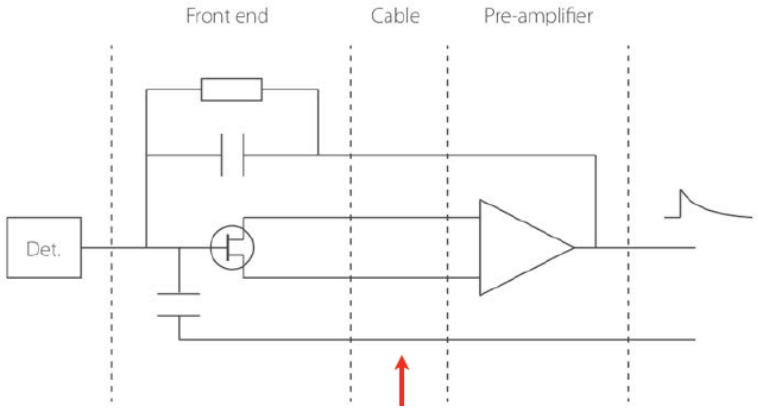


~1pF for 1kg crystal

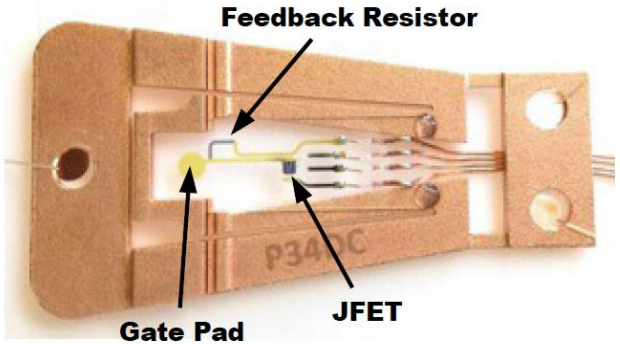
CJPL

高纯锗探测器的读出

- 低能量阈值 → 低噪声
- 低本底 → 低物质量和“干净”的材料
- 直接浸泡在液氮中→工作在77K低温
- 同时探测暗物质和0vbb→宽动态范围
- 通常高纯锗探测器采用具有较低的1/f噪声的JFET读出



~1m, increases as detector array scales

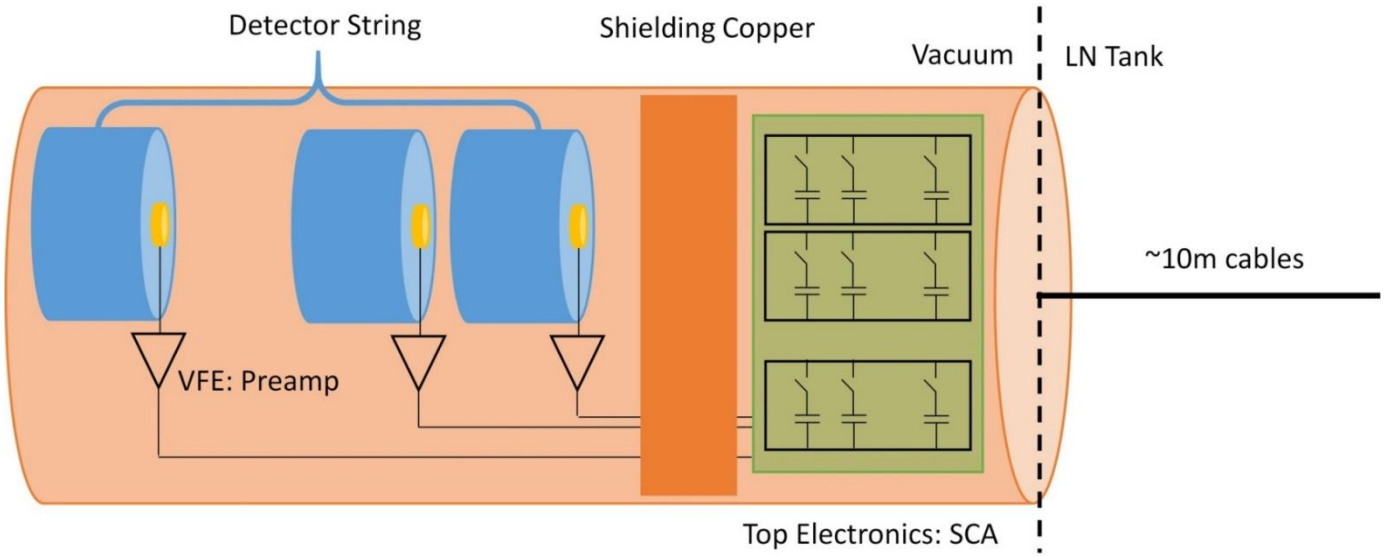


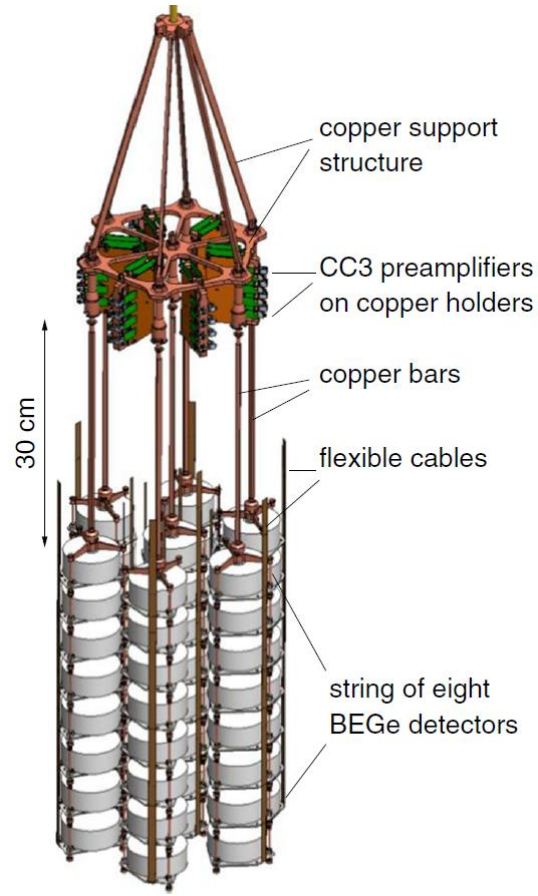
MAJORANA Demonstrator

CJPL

高纯锗探测器的读出

- CMOS ASIC具有集成度高、可定制化等特点，并且可以直接浸泡在液氮中，适合大规模阵列实验
- 基于CMOS ASIC的低温读出电子学方案



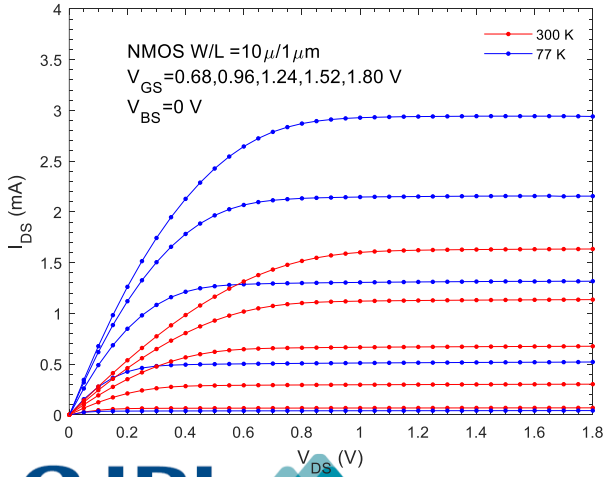


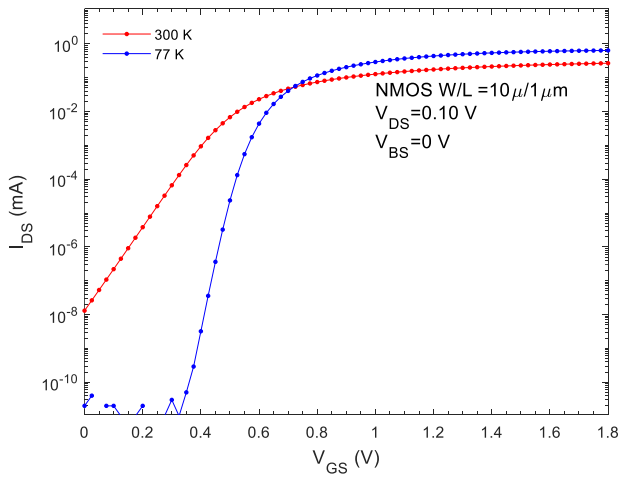
CJPL

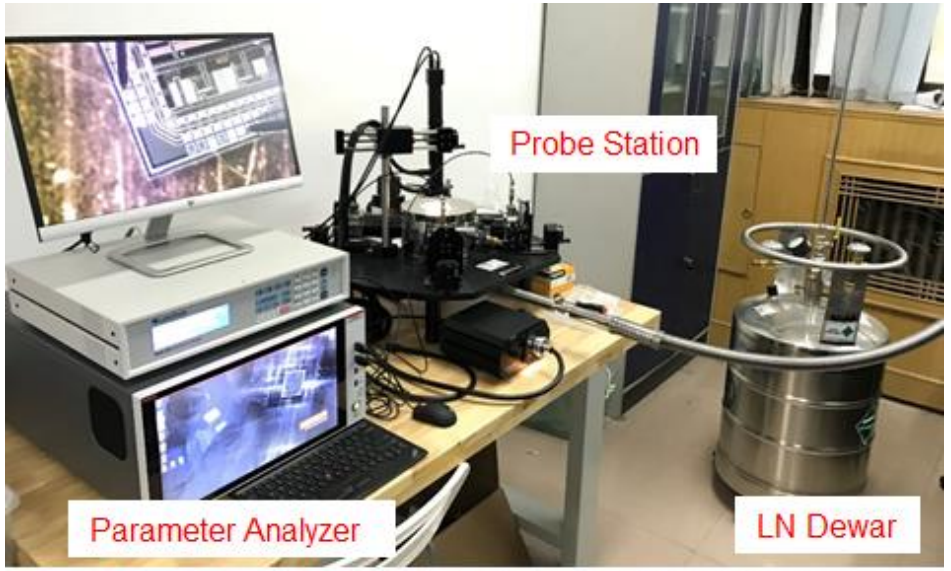
低温MOS晶体管模型

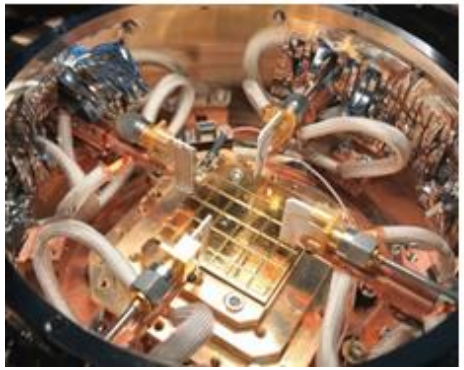
- 低温晶体管I/V测试

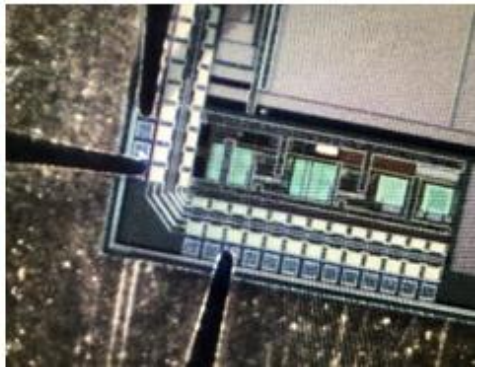
TYPE	Parameter
Process	GF 0.18 μm CMOS
Temperature	77 K, 300 K
n- and *p*-channel MOSFETs	10 μm /1 μm
	10 μm /10 μm
	10 μm /0.35 μm
	0.22 μm /10 μm







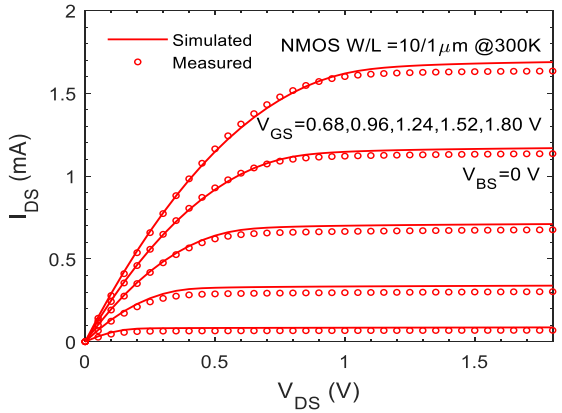


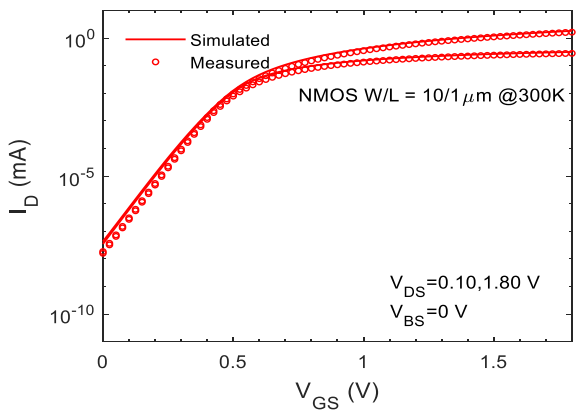


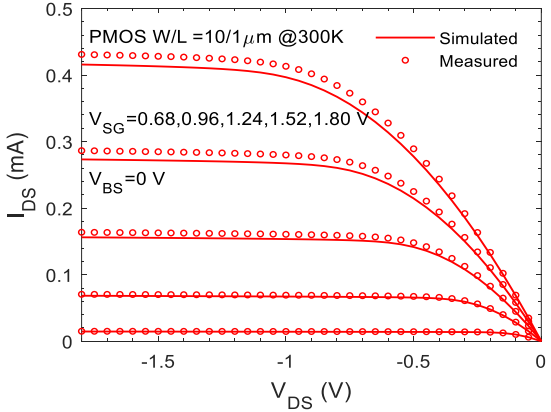
CJPL

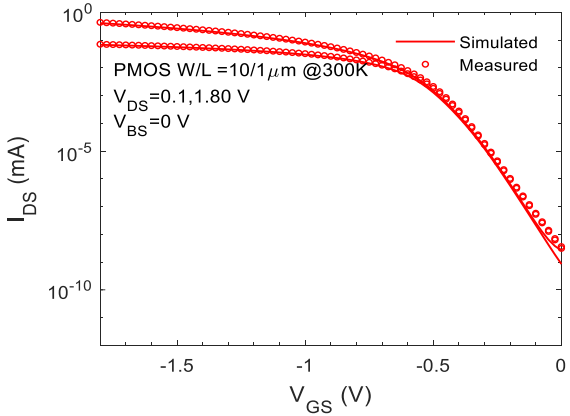
低温MOS晶体管模型

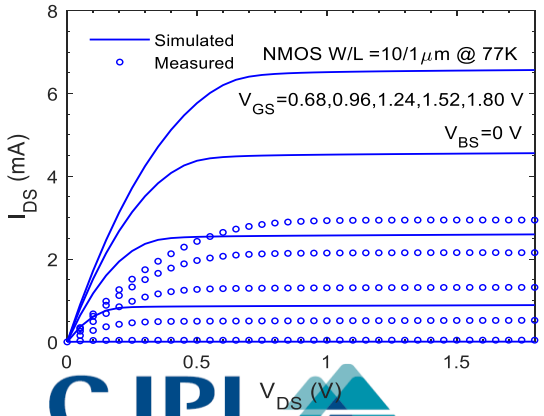
- 标准BSIM模型只适用于220K以上的温度

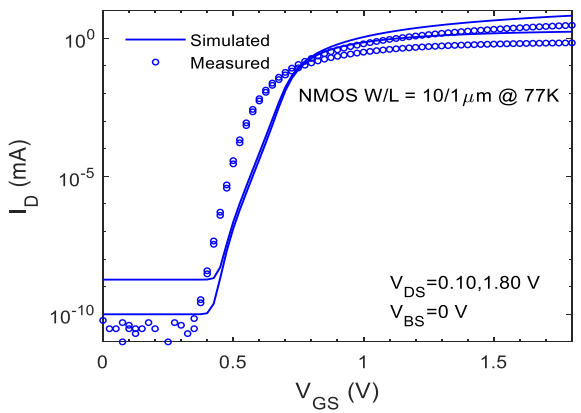


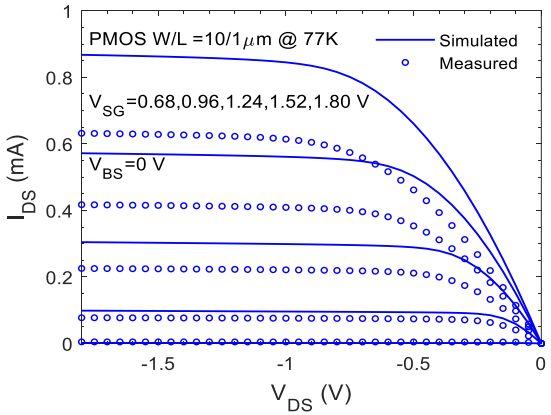


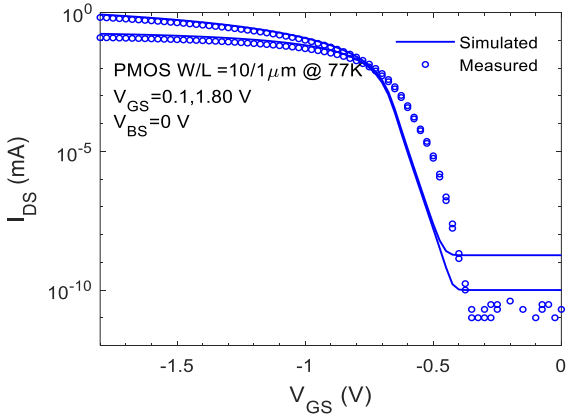










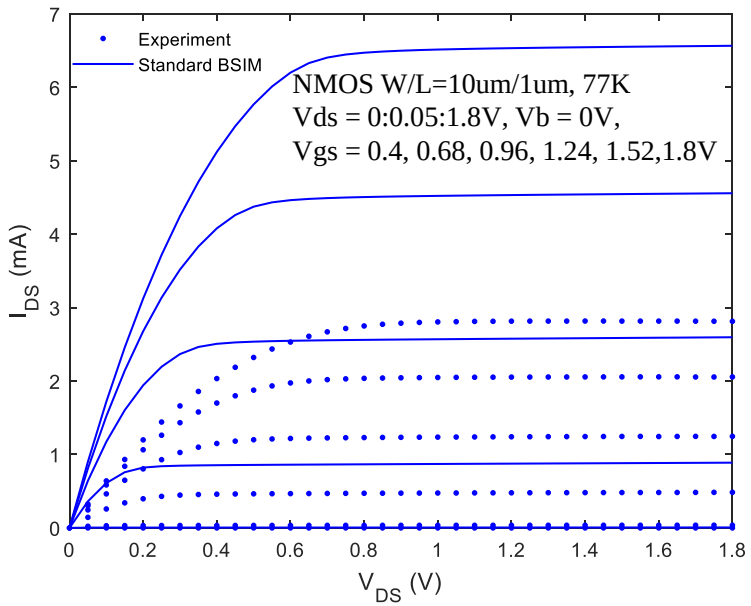


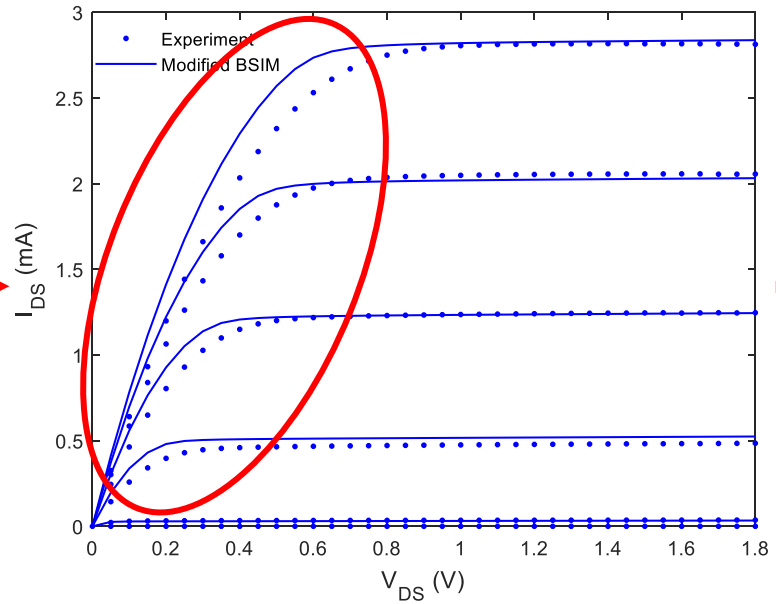
CJPL

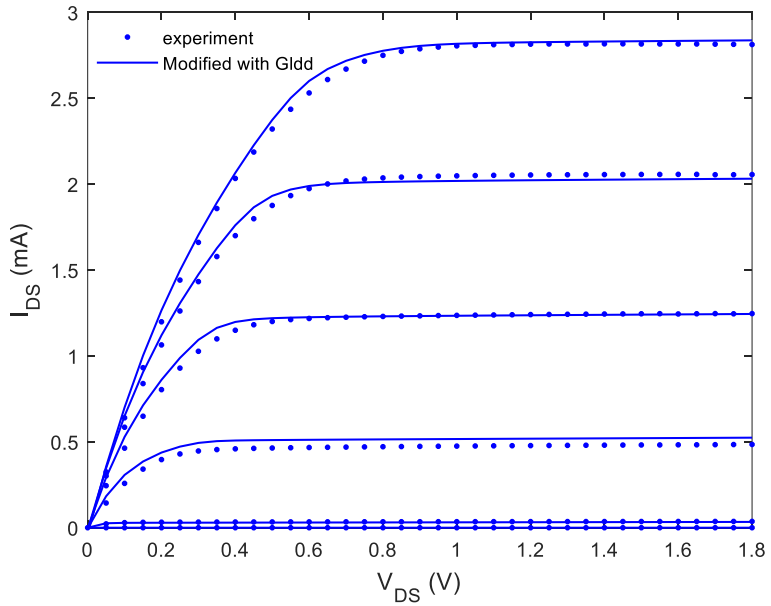
低温MOS晶体管模型

- 通过微调BSIM模型中阈值（kt1）、迁移率（ute）、饱和速度（at）等参数
- 迭代得到最小误差

$$error = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\frac{I_{dsim} - I_{dmea}}{I_{dmea}}\right)^2} \times 100\%$$





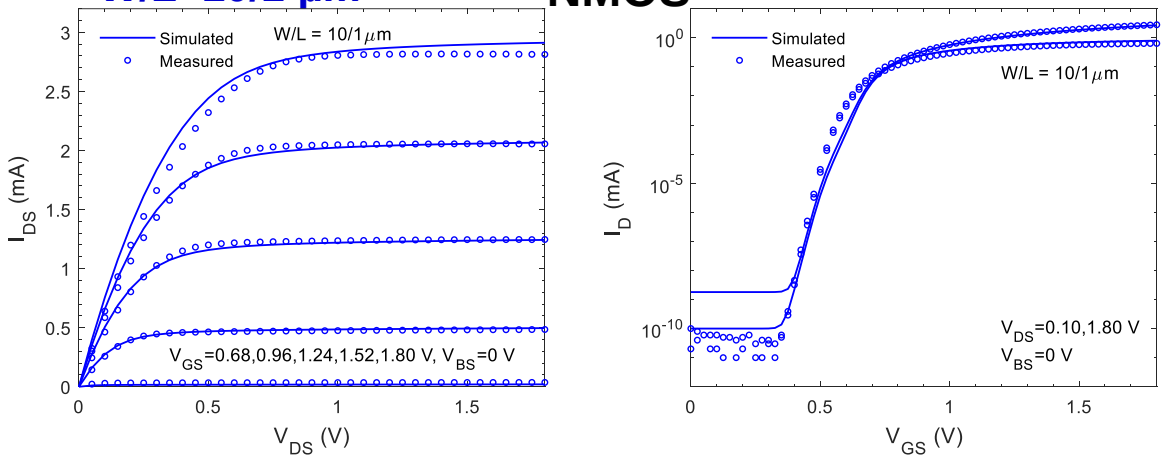


CJPL

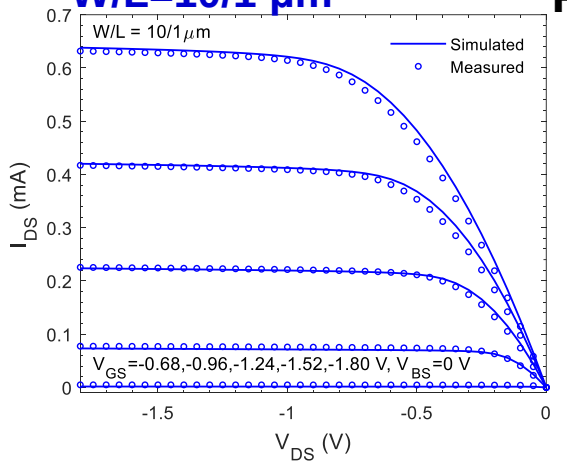
低温MOS晶体管模型

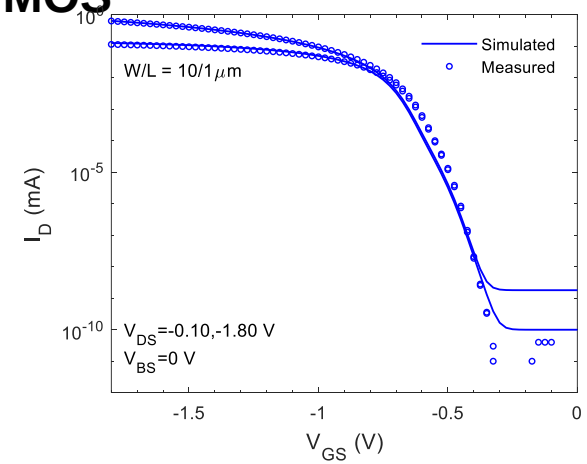
- 修改模型参数后不同尺寸晶体管的IV曲线，仿真与实测值误差<10%

W/L=10/1 μm **NMOS**

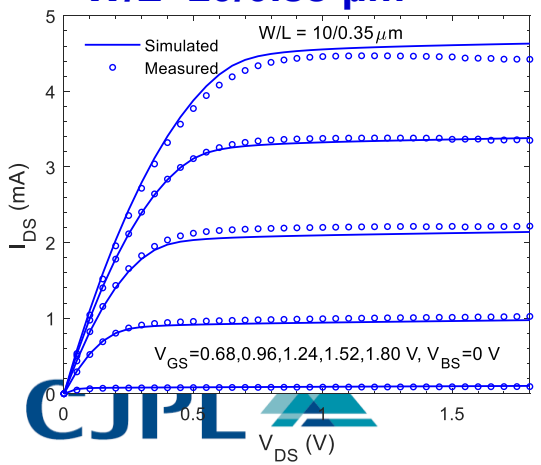


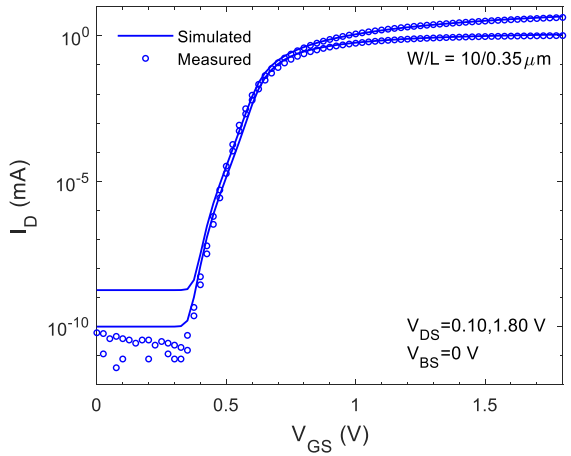
W/L=10/1 μm **PMOS**



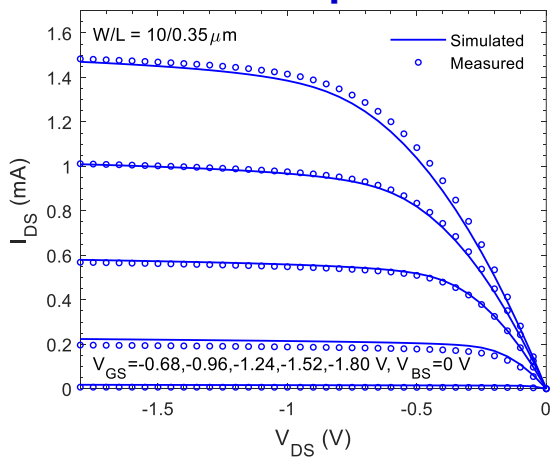


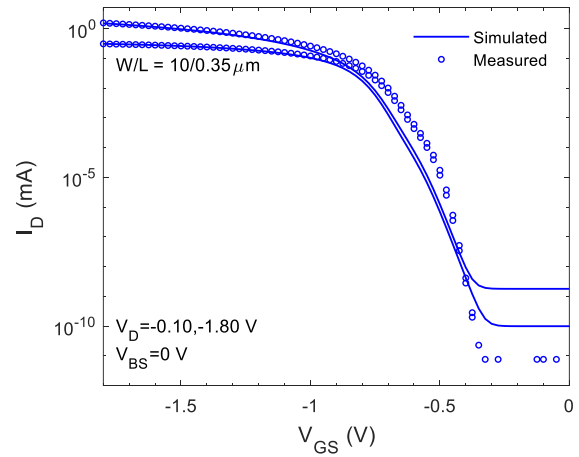
W/L=10/0.35 μm



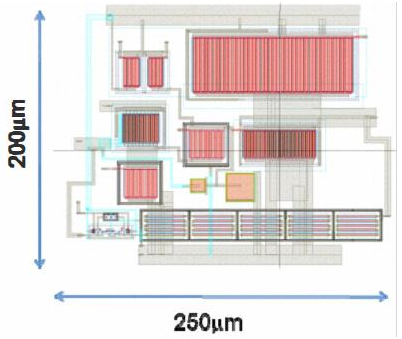


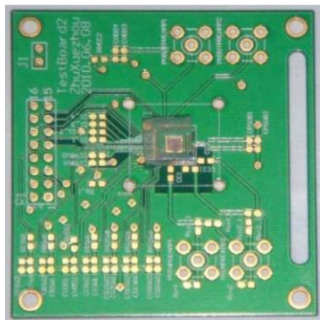
W/L=10/0.35 μm



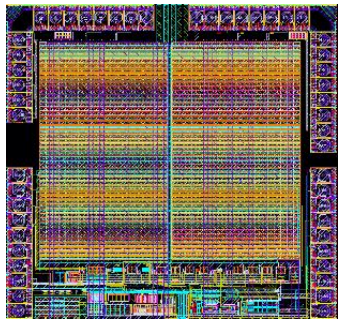


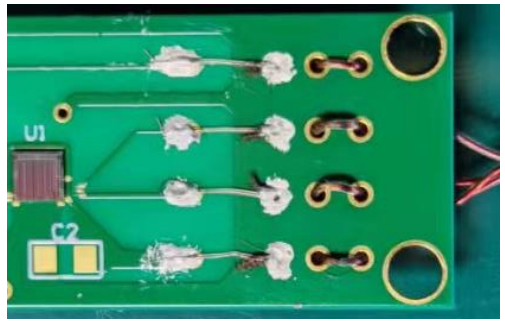
低噪声CMOS前放ASIC





工艺	GF 350nm
ENC	6.5 e⁻ @ 213K 12μs
能量分辨率	3.9 keV @ 662 keV

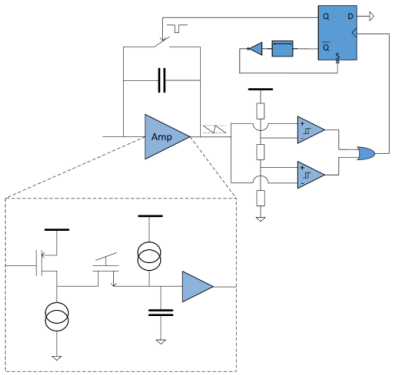


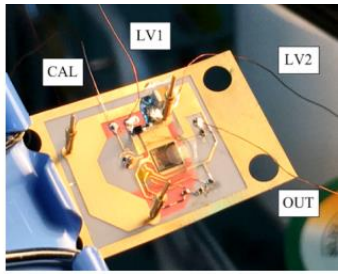


工艺	XFAB 350nm
ENC	8.9 e⁻ @ 77K 12μs
能量分辨率	600 eV @ 122 keV

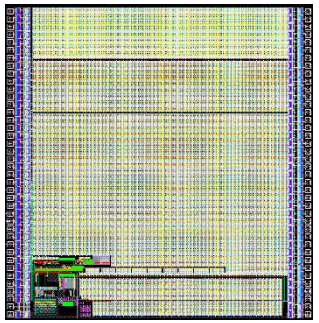
2011 2018 2021 2022

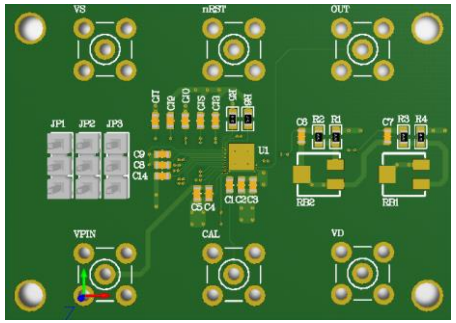
最新版正在测试





工艺	GF 350nm
ENC	9.7 e⁻ @ 77K 12μs
能量分辨率	640 eV @ 122 keV



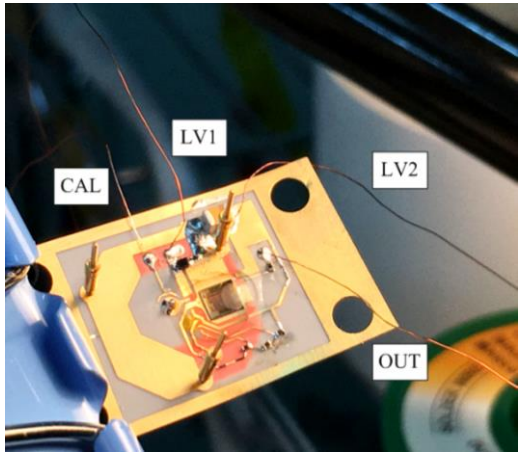


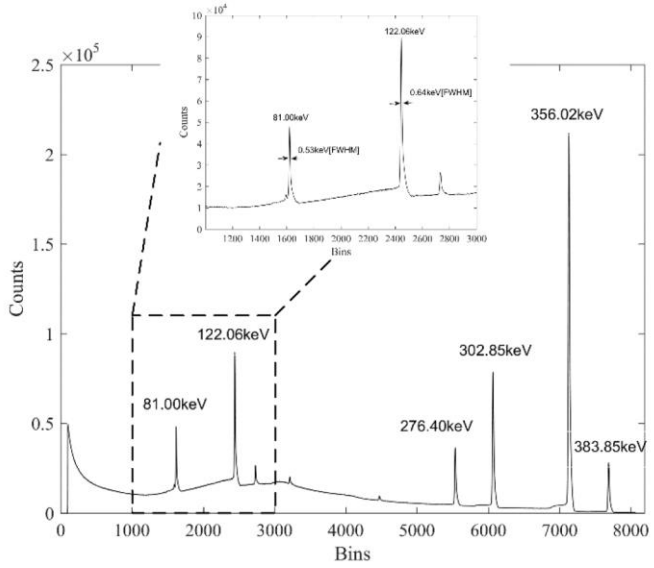
工艺	GF 180nm
ENC	待测
能量分辨率	待测

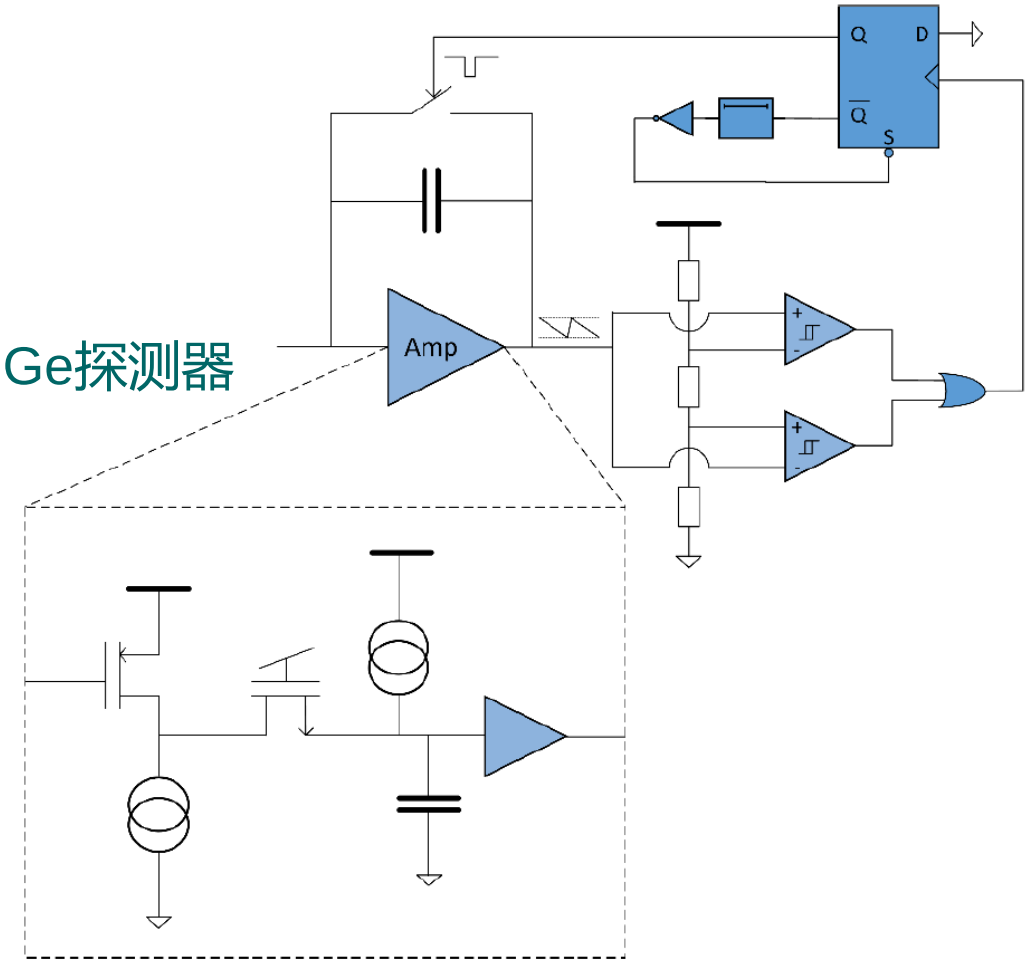
CJPL

低噪声CMOS前放ASIC

- 2018年：
  - 采用0.35um CMOS工艺
  - 脉冲复位
  - 增益：5-20 mV/fC
  - ENC噪声：13.3 e @ 2pF, 77K, 26 e @ 0.5kg HPGe探测器





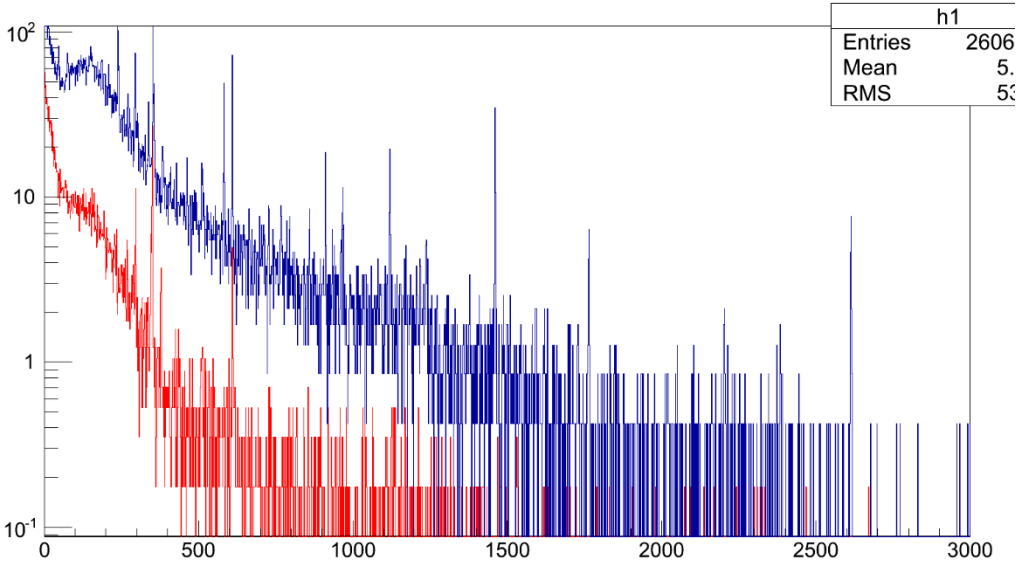


Z. Deng, et. al. JINST P08019 2018

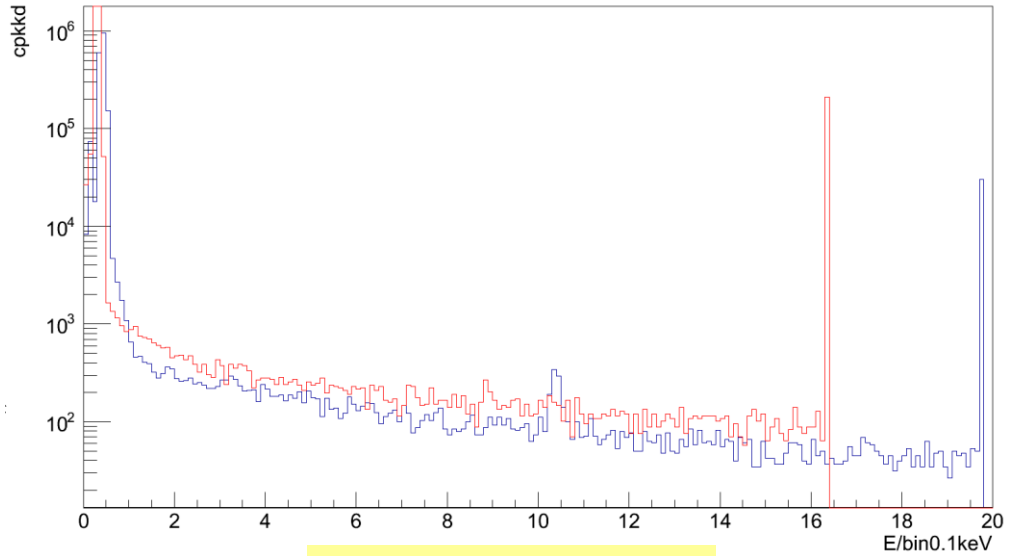
CJPL

在 CDEX 实验中的应用

- 在CJPL开展的部分实验工作



高能区本底分析

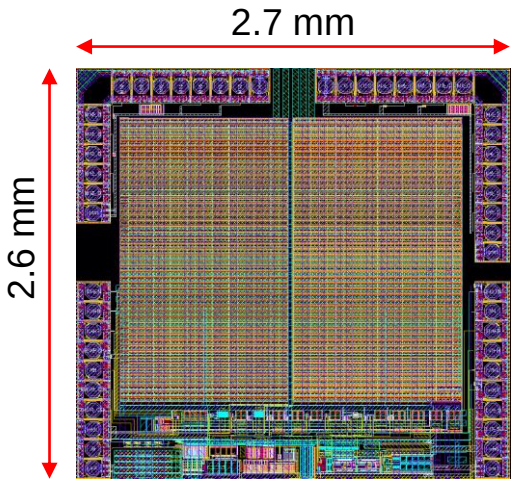


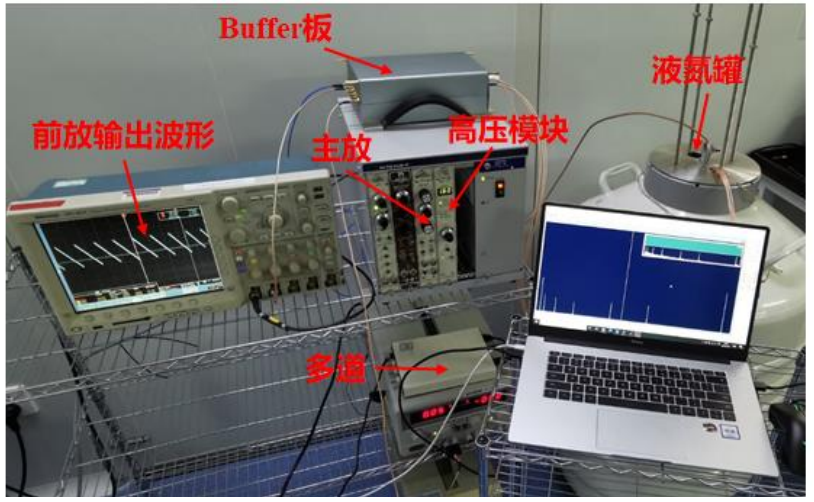
低能区本底分析

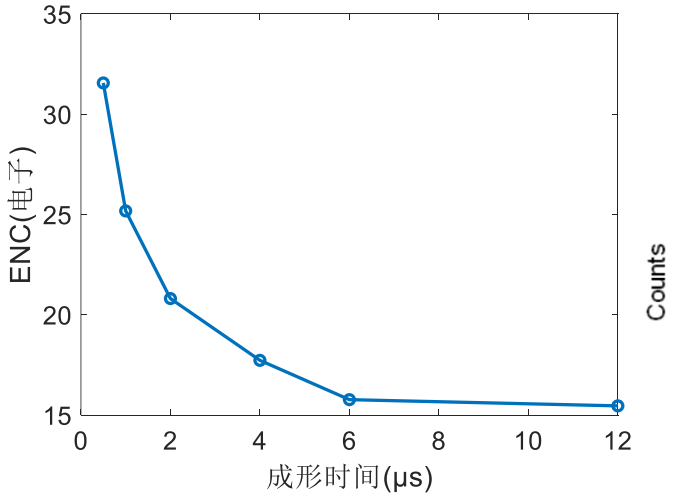
CJPL

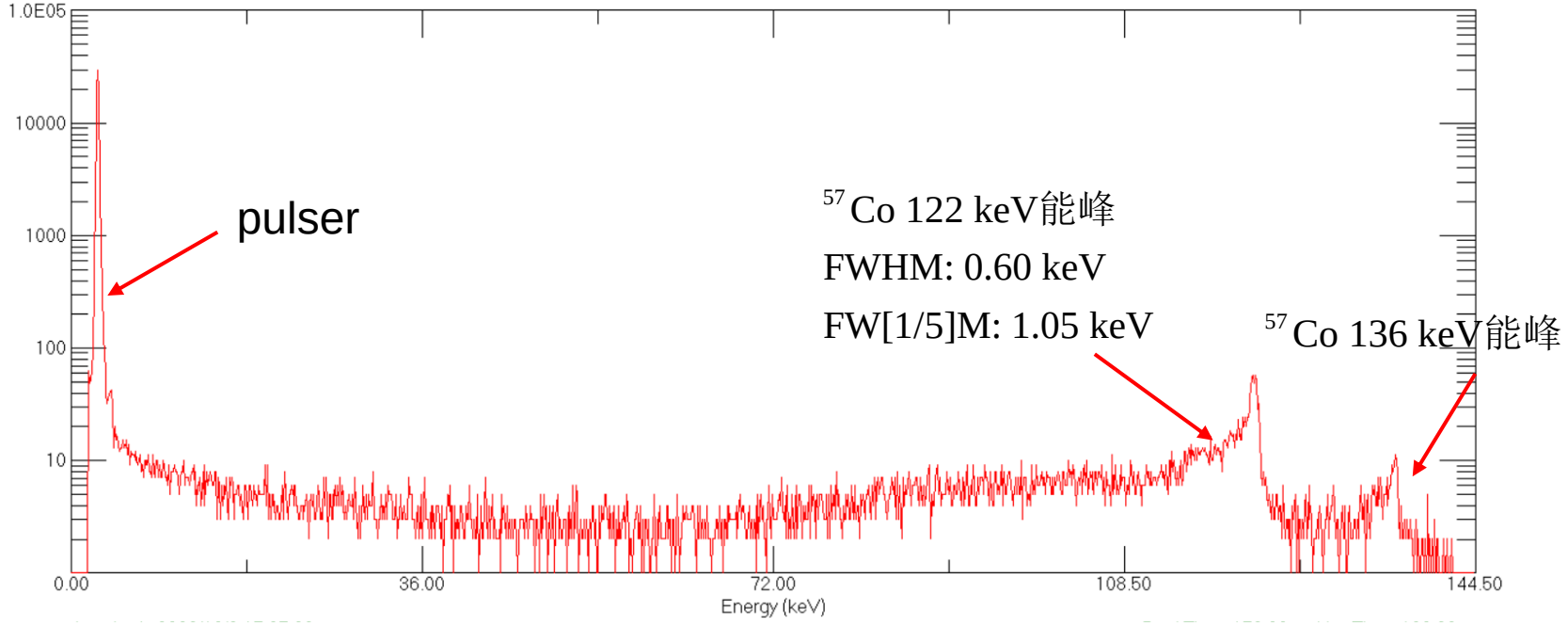
低噪声CMOS前放ASIC

- 2021年
  - ENC=15.5 e @ 0.5kg HPGe，目前CMOS前放ASIC连接大探测器的最好噪声结果







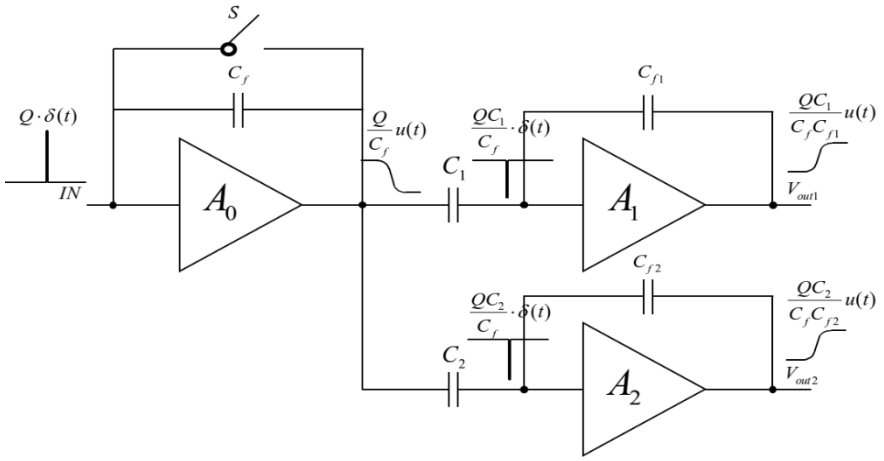


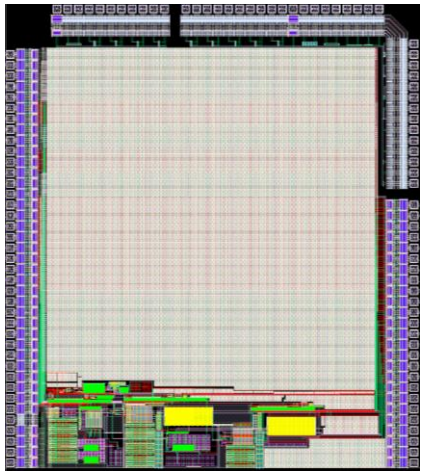
CJPL

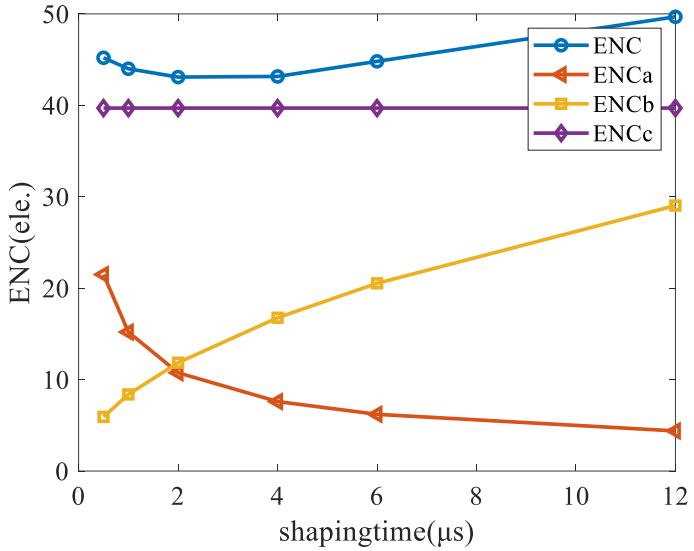
宽动态CMOS前放ASIC

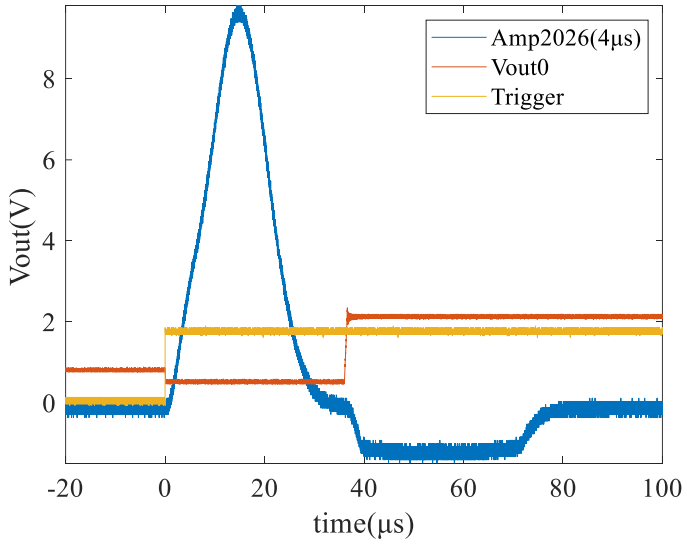
- 同时探测暗物质与无中微子双β衰变
  - 暗物质感能区：0 - 20 keV
  - 无中微子双β衰变能区：5 MeV
- 双增益+提前复位

DR >100000 : 1





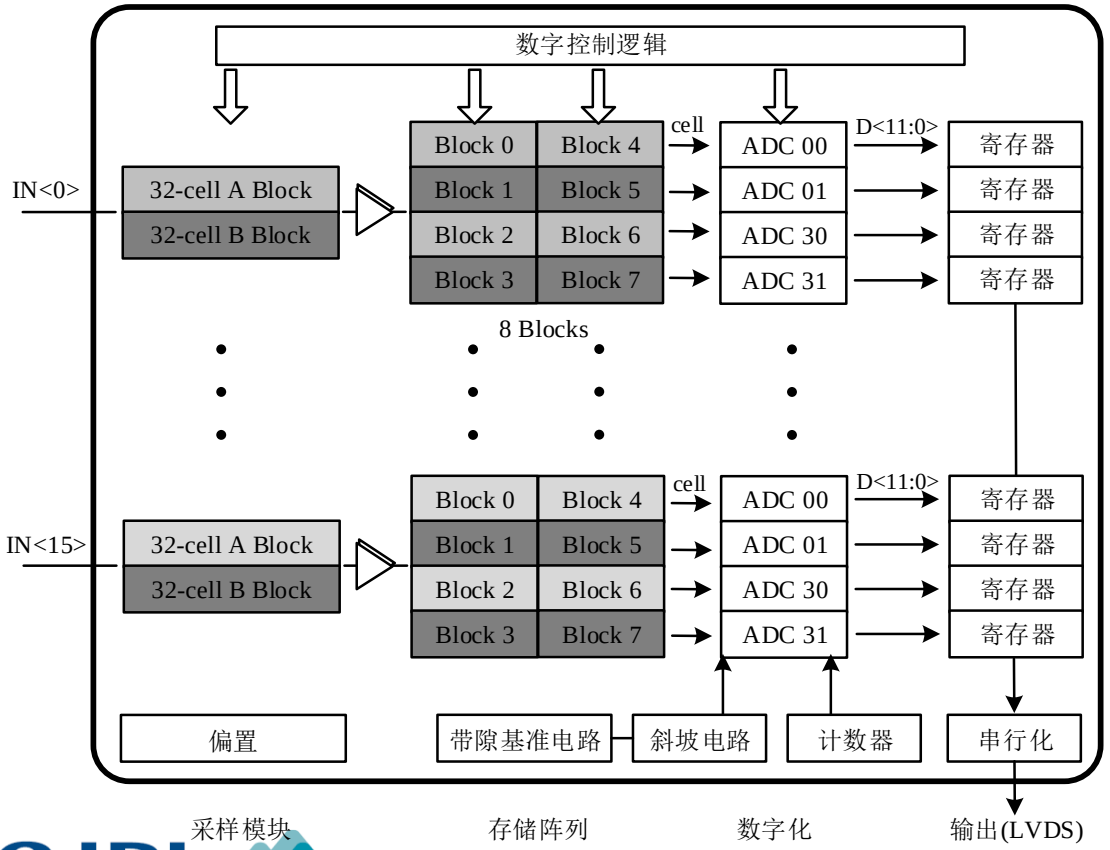




CJPL

低温SCA波形采样ASIC

- 基于SCA（开关电容阵列）的波形采样芯片

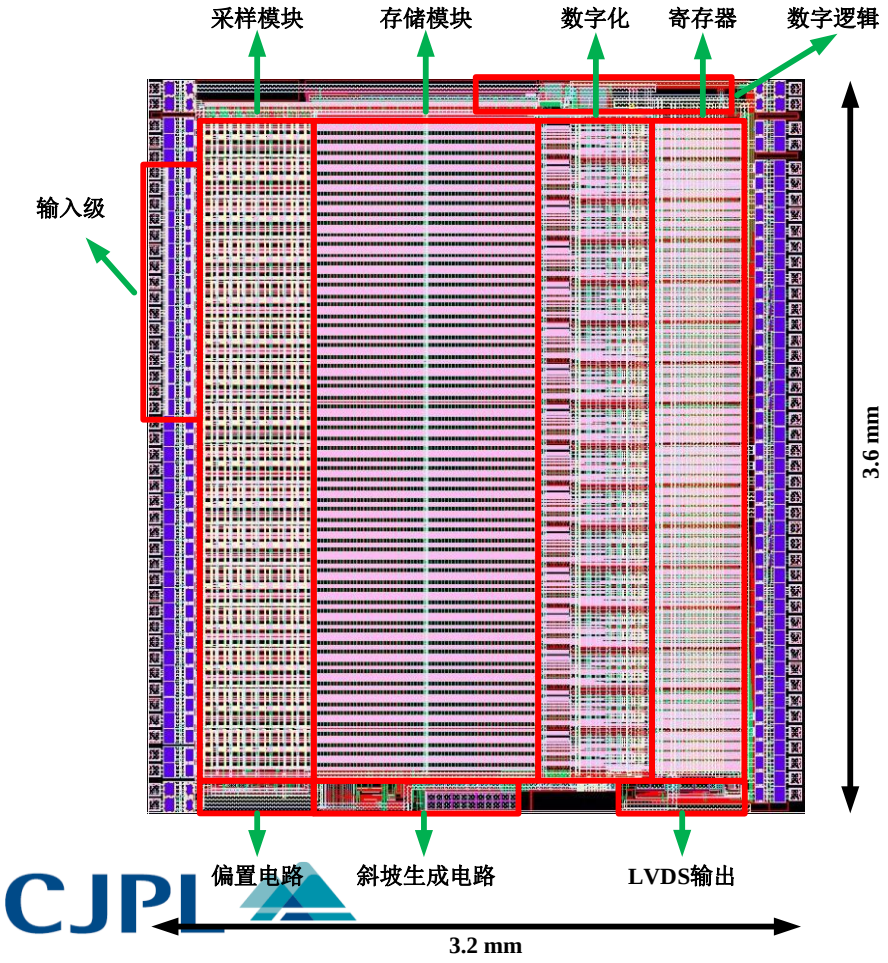


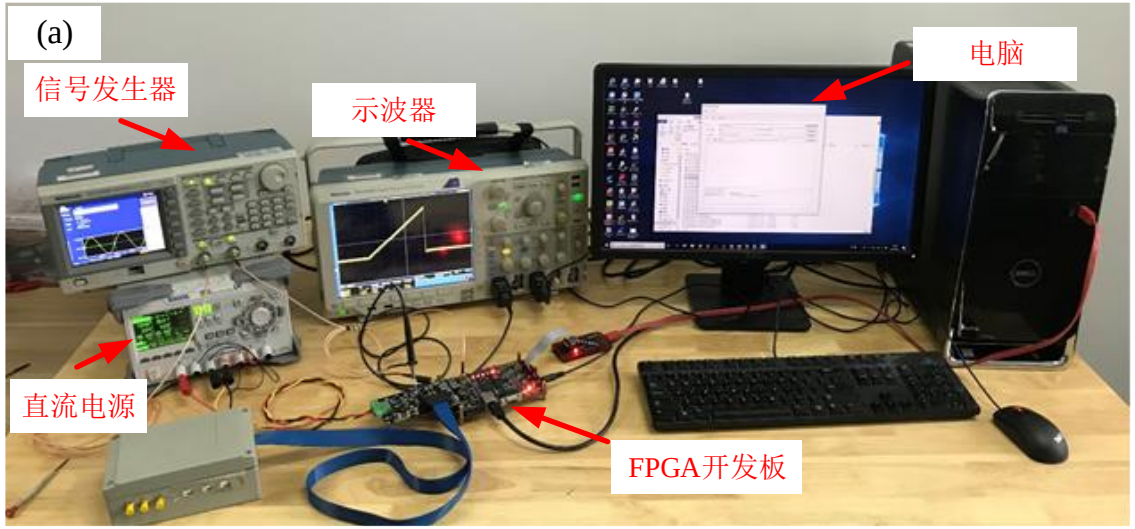
参数	指标
工艺	0.18 μm CMOS 工艺
工作电压	1.8 V，2.5 V
输入动态范围	0.3V - 1.3 V
采样频率	100 MS/s
采样深度	32 - 256
采样精度	> 10 bits
ADC时钟频率	100 MHz
ADC计数器	12 bits
ADC转换时间	42 μs
最大死时间	336 μs
核心功耗	3.2 mW/ch

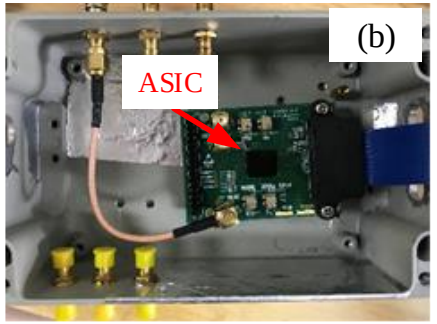
CJPL

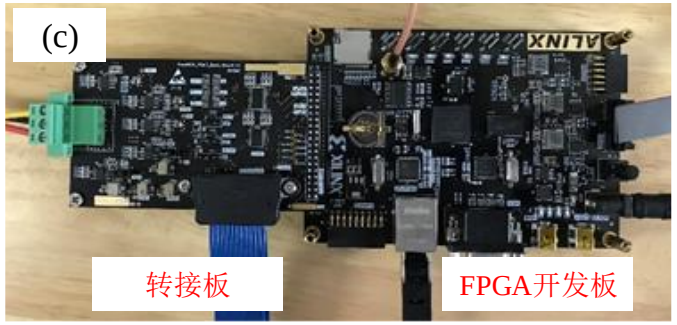
低温SCA波形采样ASIC

- 芯片版图和测试装置





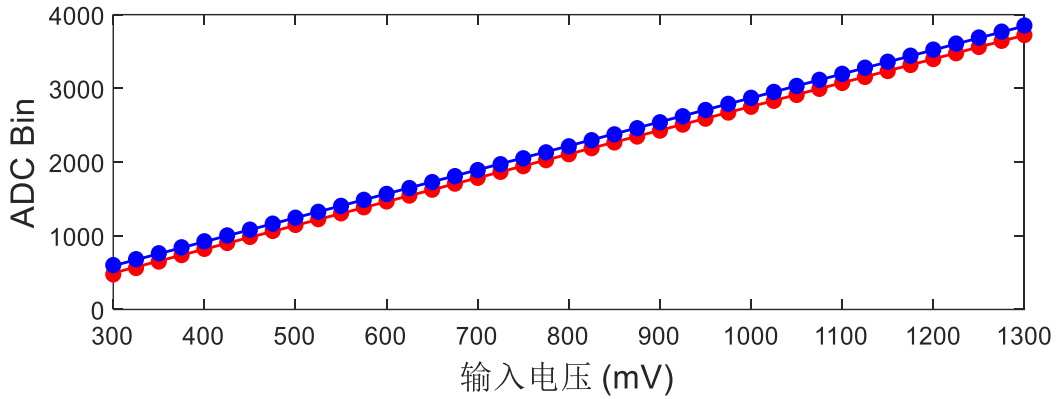


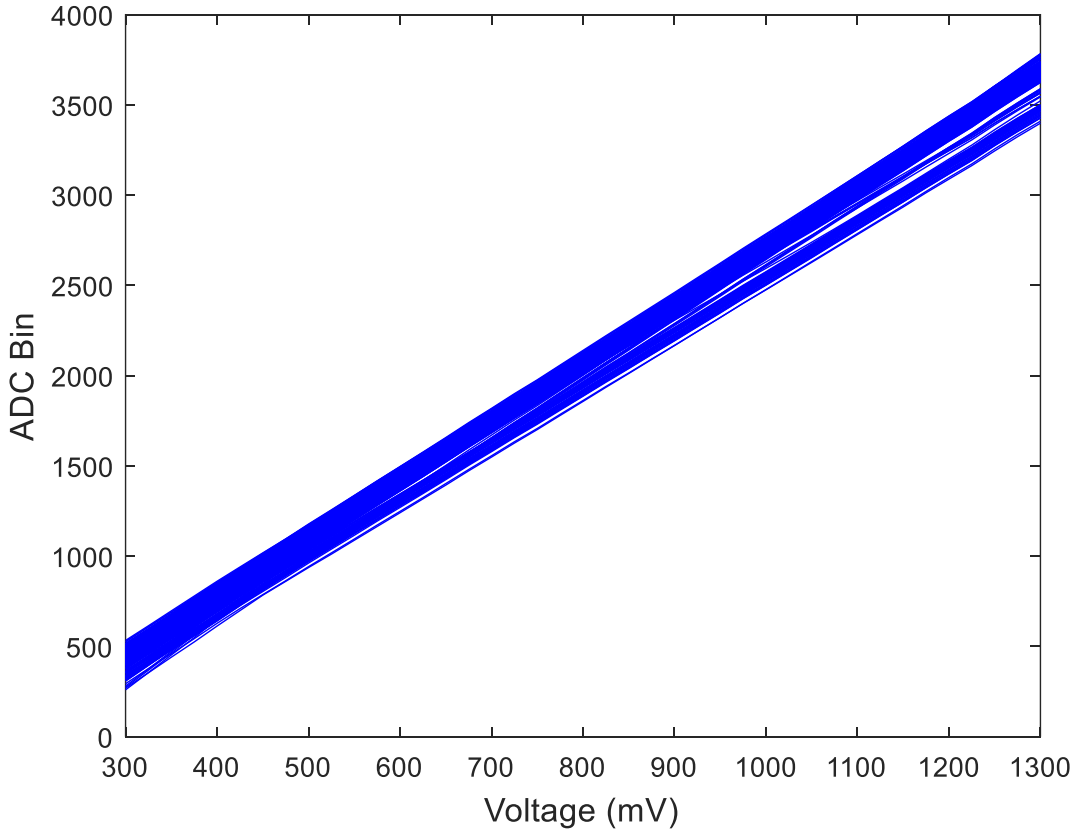


低温SCA波形采样ASIC

- 积分非线性

0.41% (室温) → 0.25% (低温)



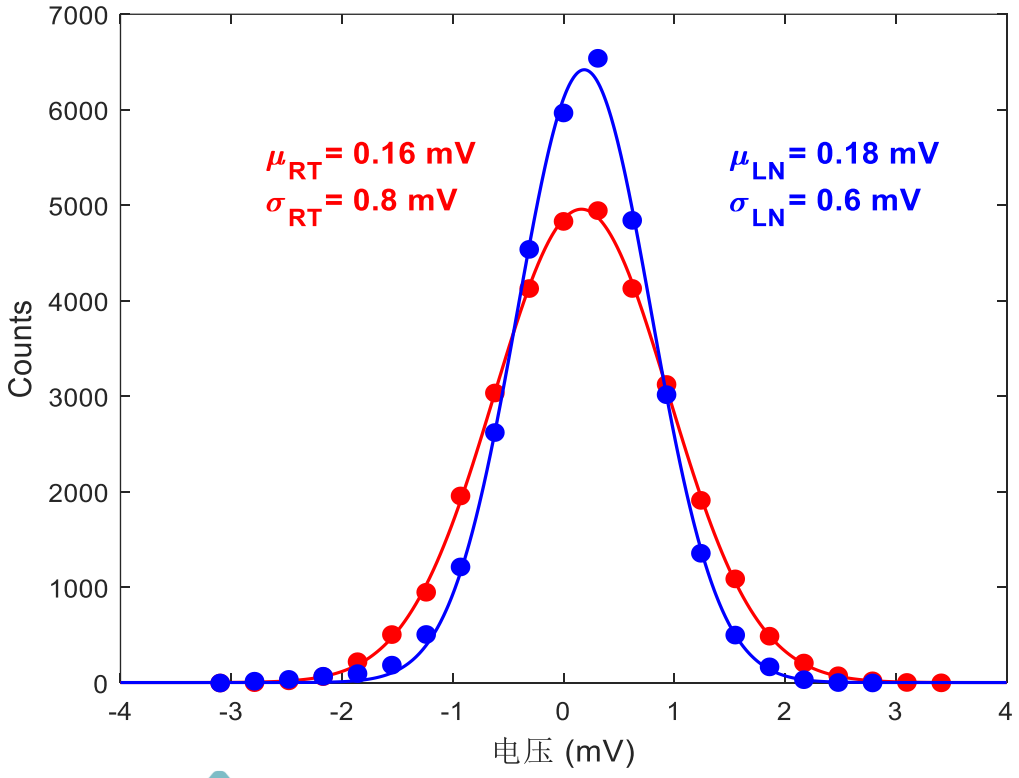


CJPL

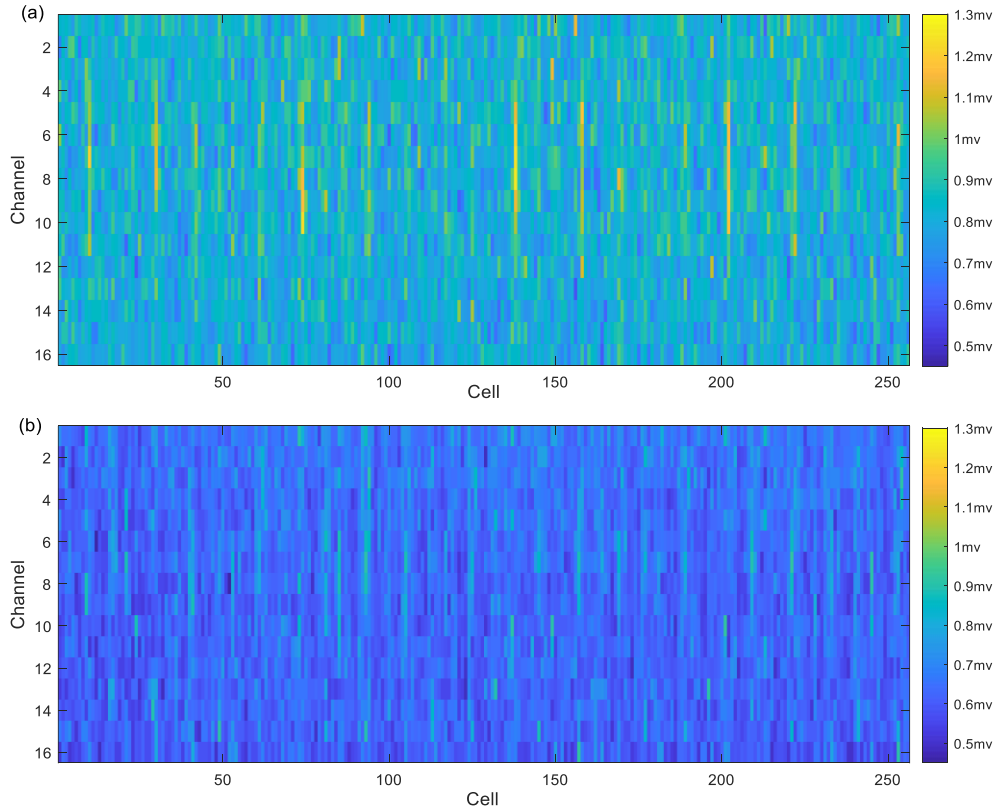
低温SCA波形采样ASIC

- 静态噪声性能

0.8 mV (室温) → 0.6 mV (低温)



全芯片噪声分布较均匀

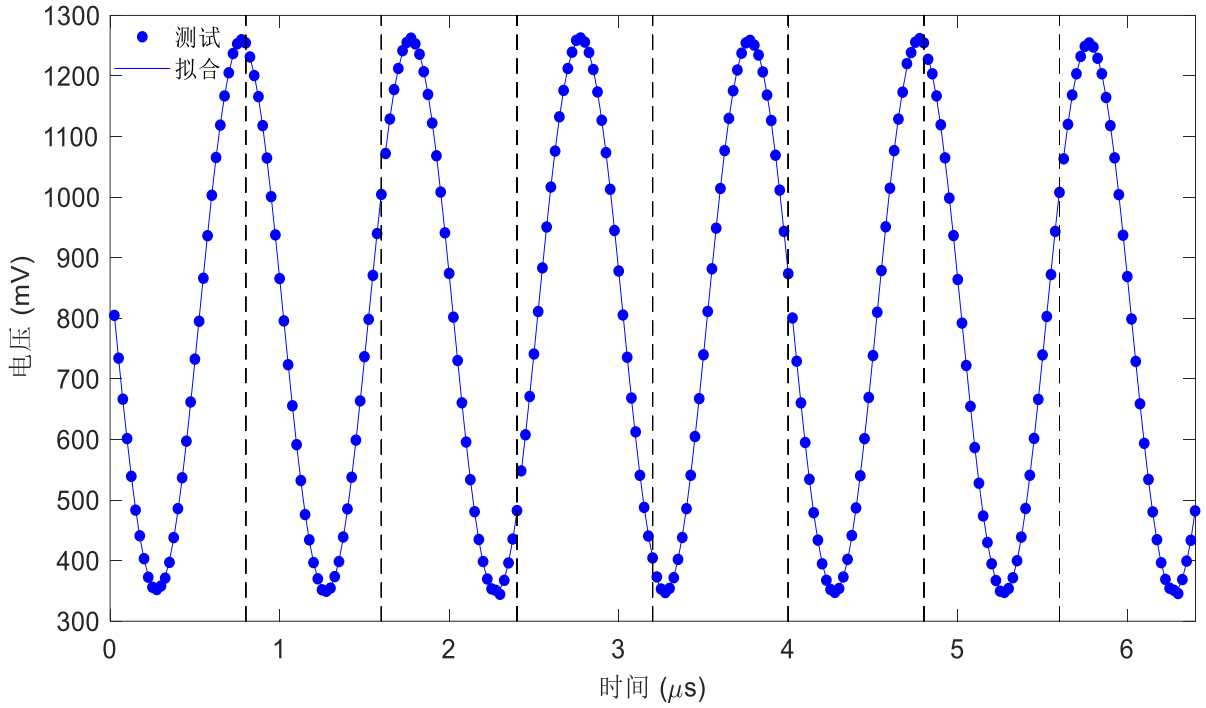


CJPL

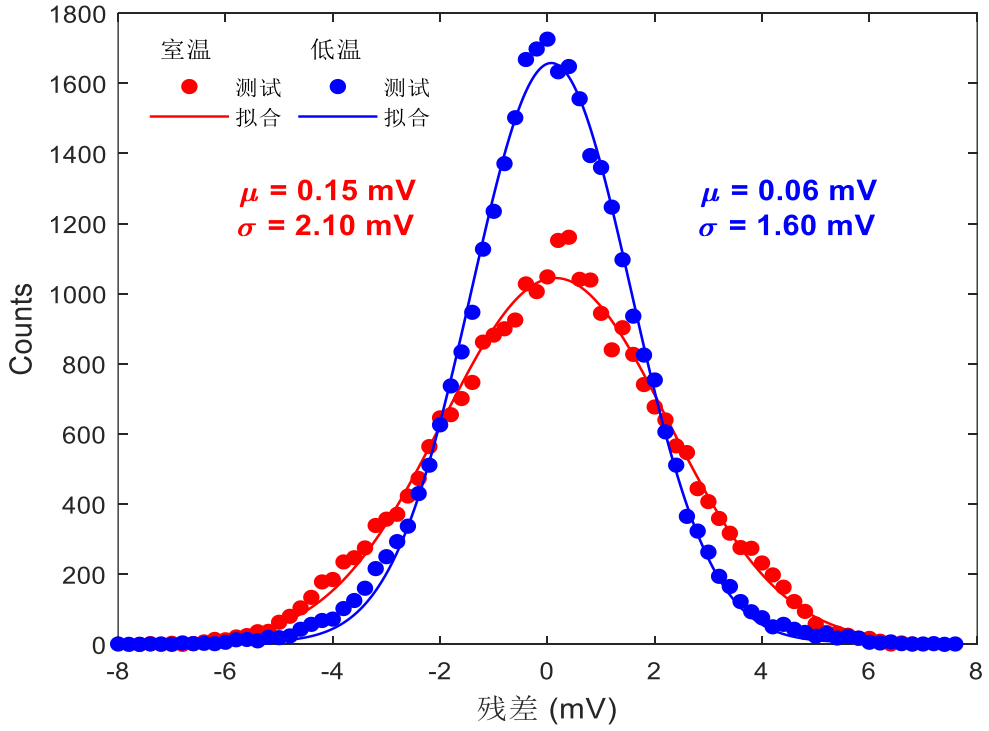
低温SCA波形采样ASIC

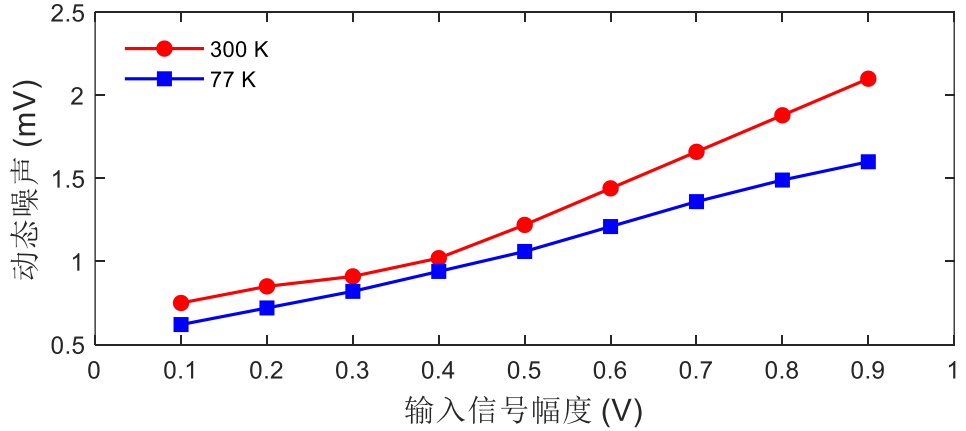
- 动态噪声性能

8.9 bits (室温) → 9.3 bits (低温)



低温40 MS/s连续采样经校准后的曲线





CJPL

小结

- 目前完成的工作
  - 补充低温（77K）下的CMOS仿真模型，根据该模型下设计出的电路仿真结果和实测结果误差 < 10%
  - 设计完成多版前端低噪声ASIC，2018版ASIC已完成在锦屏的初步测试工作，2021版（本底更低）ASIC正在配合测试
  - 能够同时应用于暗物质与0Vββ衰变实验中的宽动态范围ASIC完成了原理验证
  - 低温SCA波形采样ASIC已完成基本性能测试
- 未来的工作计划
  - 2021版（低本底版）ASIC配合完成CDEX相关实验验证工作；
  - 完成宽动态范围ASIC的设计以及配合进行实验；
  - 应用低温SCA波形采样ASIC到实验测试中；
  - 更低噪声的ASIC设计：进一步降低1/f噪声。

CJPL