Design and Production of Readout Electronics for the 20-inch PMTs of JUNO experiment

Jun Hu

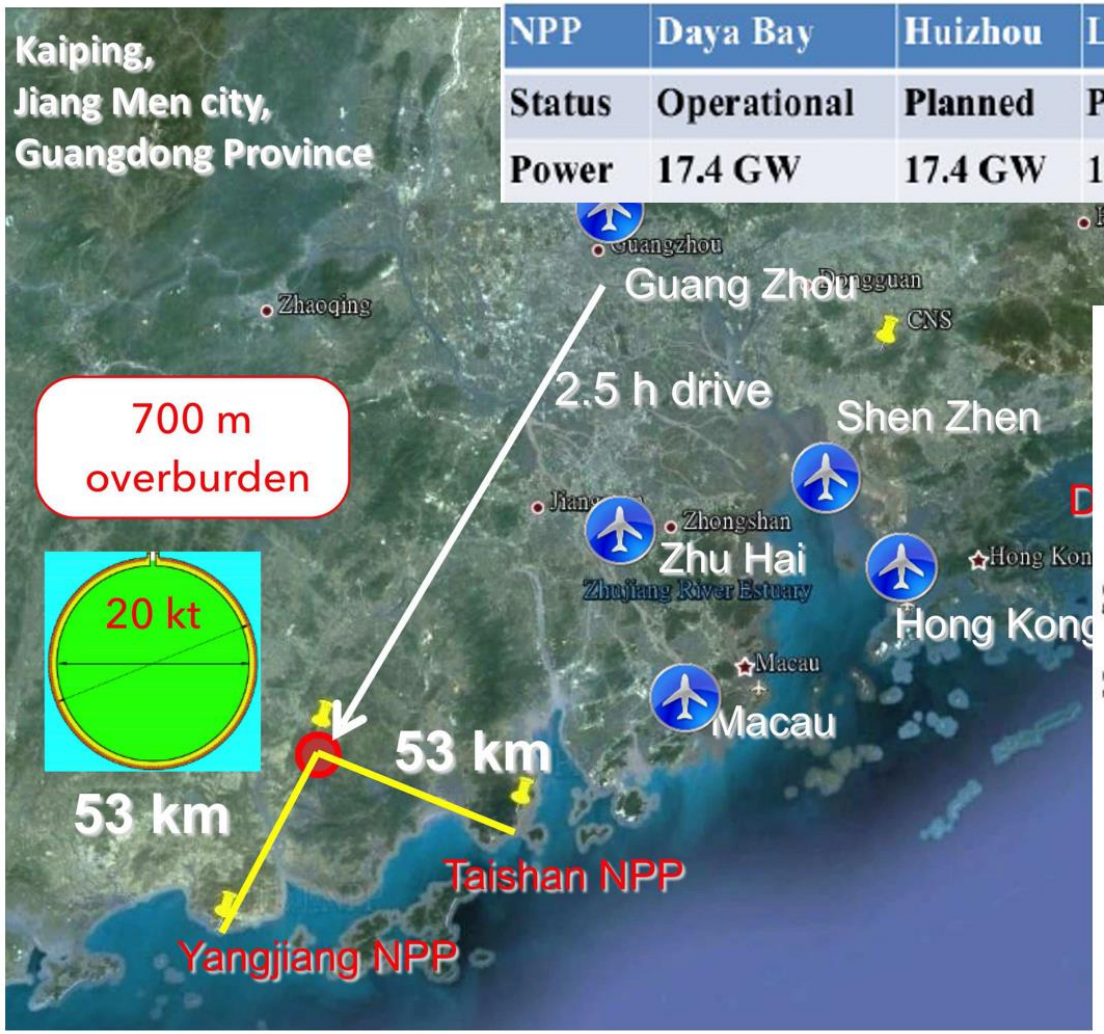
IHEP, CAS

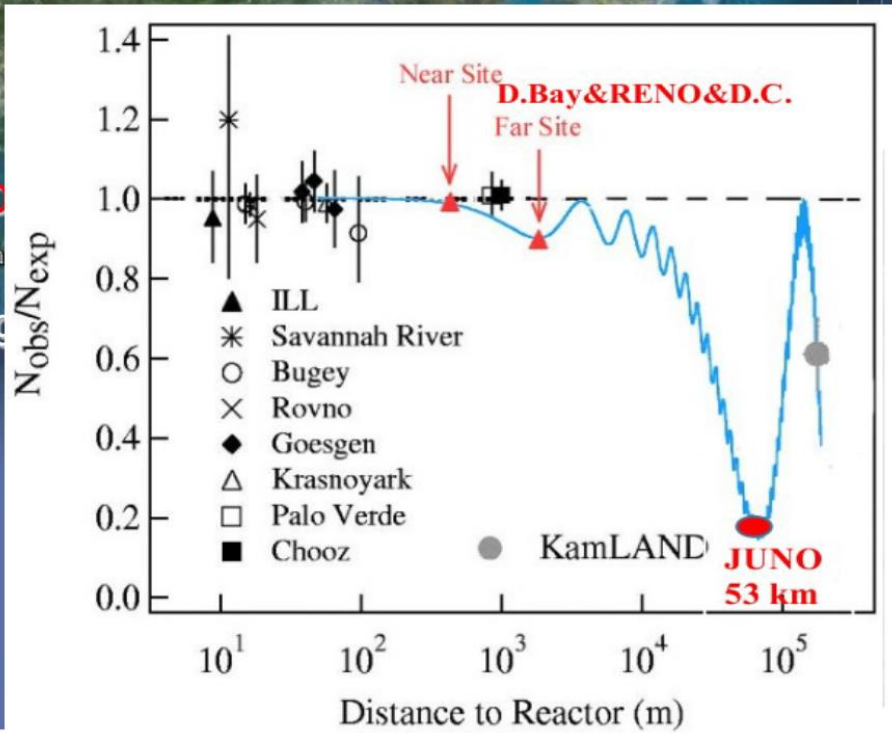
On behalf of LPMT Electronics Group

2024.5.9

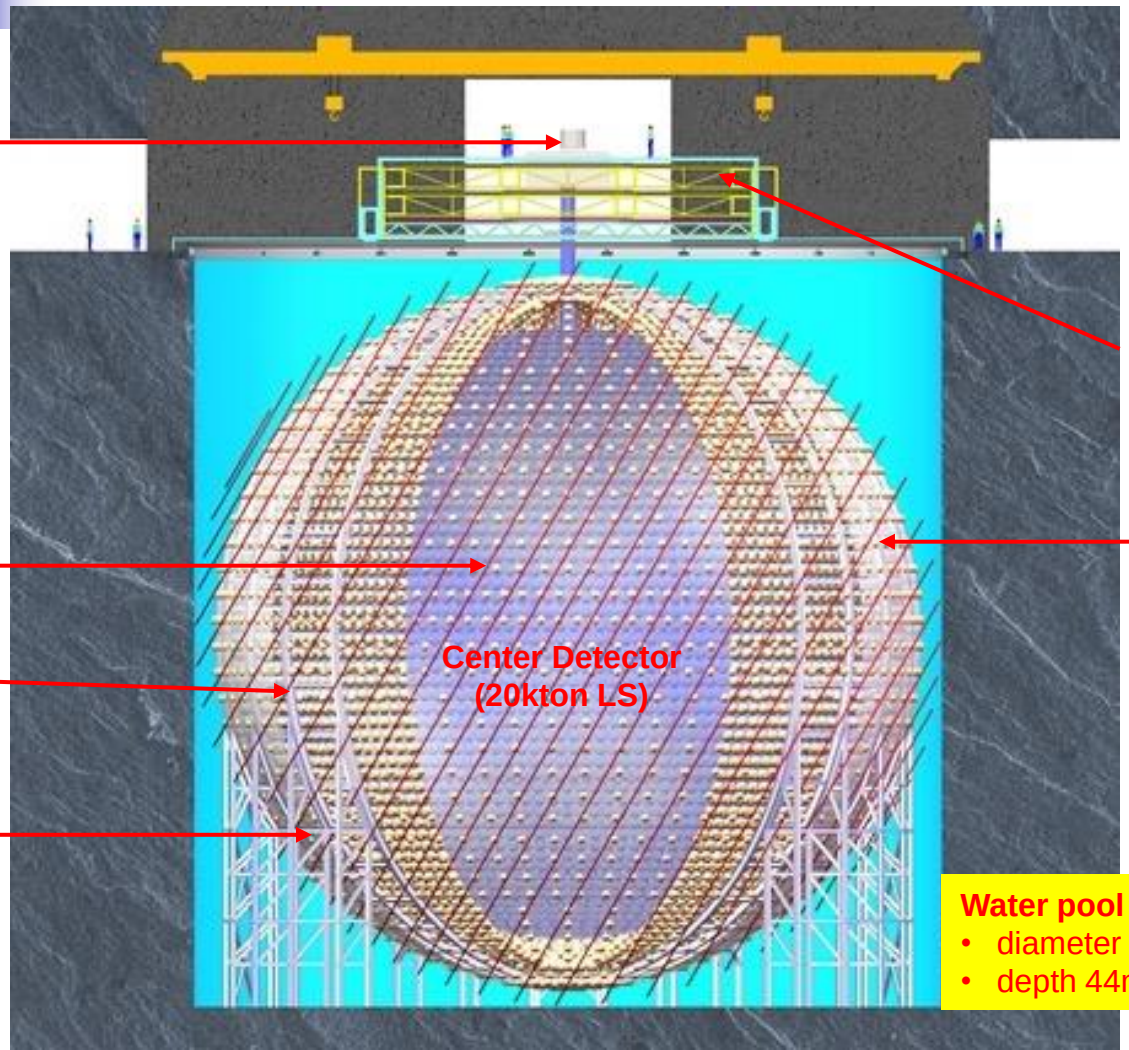
JUNO experiment (Jiangmen Underground Neutrino Observatory)

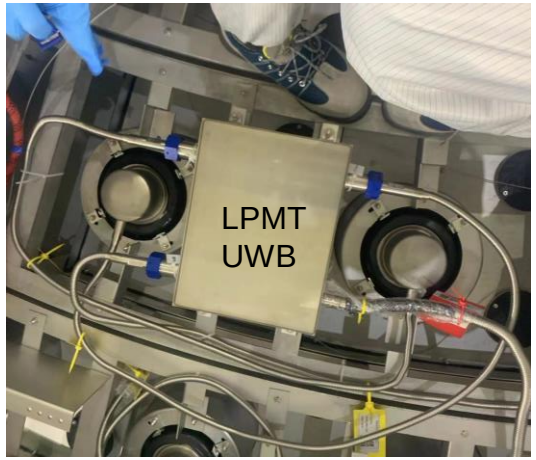
NPP	Daya Bay	Huizhou	Lufeng	Yangjiang	Taishan
Status	Operational	Planned	Planned	Operational	Operational / Planned
Power	17.4 GW	17.4 GW	17.4 GW	17.4 GW	9.2 GW / 18.4 GW



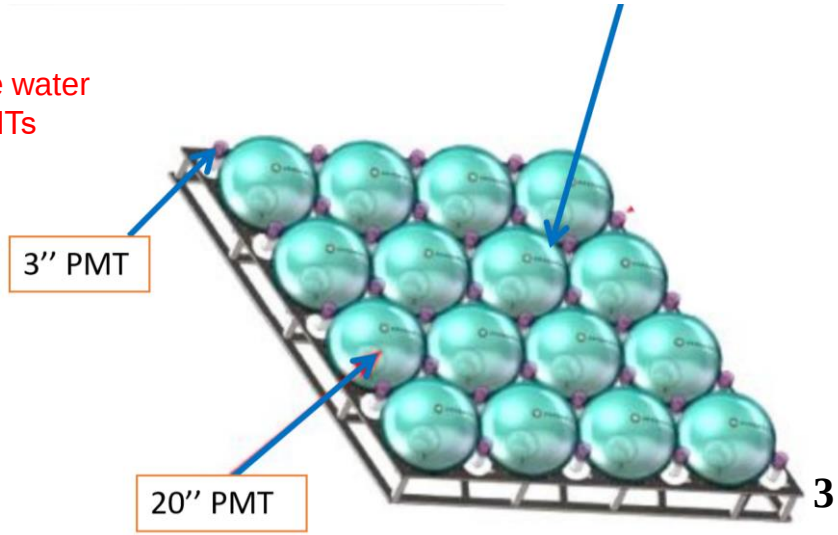


The JUNO detector





MCP-PMT

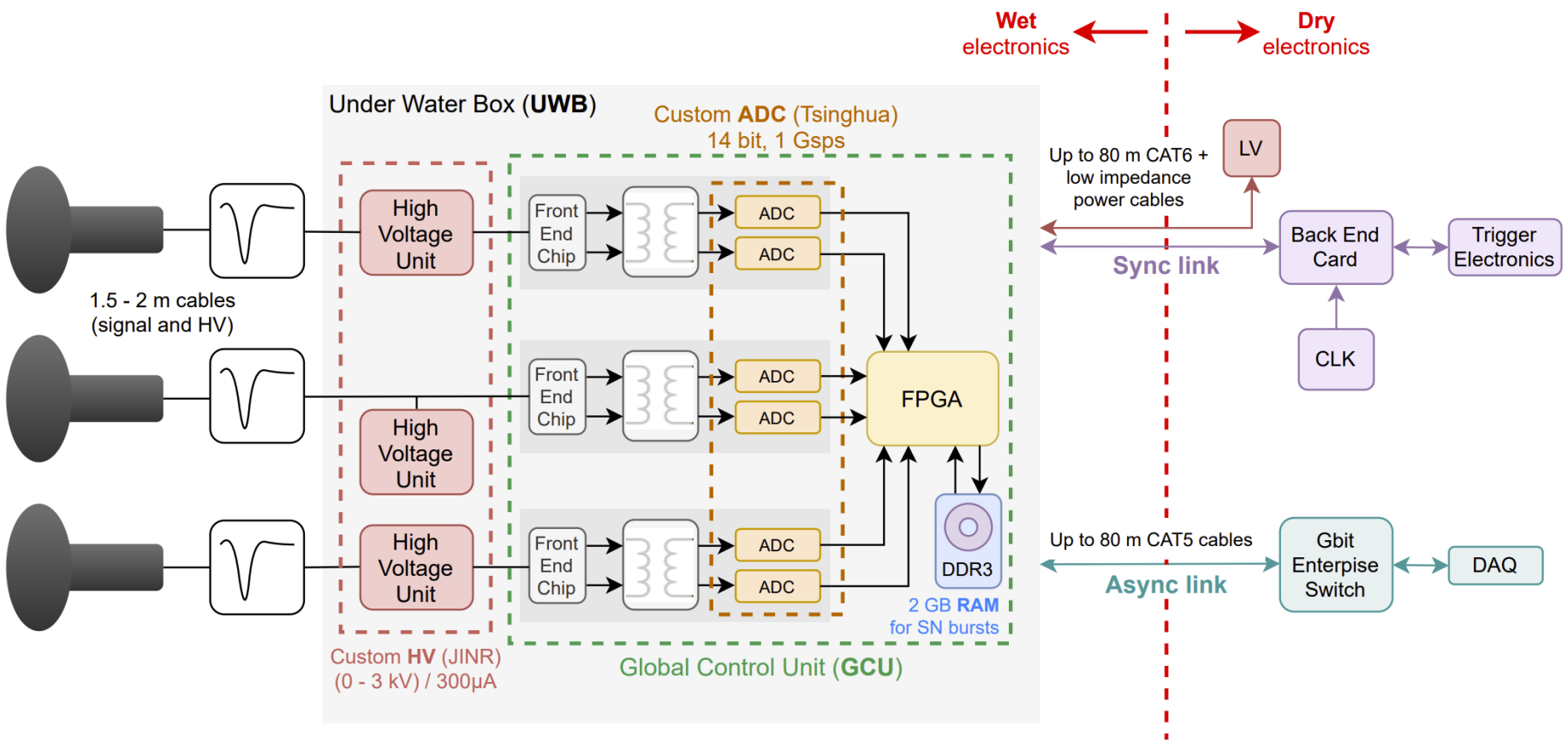


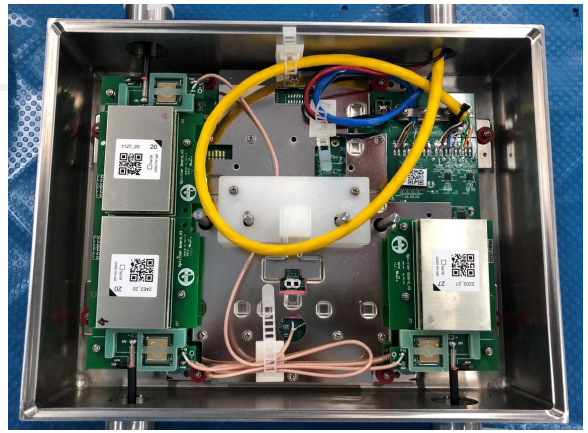
JUNO LPMT electronics Specification

- Main challenges:
  - Excellent energy resolution: 10% @ 1-100 pe, 1% @ >100 pe
  - Excellent photon arrival time measurement
  - A large dynamic range: 1-4000 pe (7.5mV-7.5V)
  - A negligible dead-time for supernova event
  - Huge number of channels: ~20000 LPMT channels
  - Aerospace-grade reliability requirements : less than 0.5% underwater electronics failure over 6 years

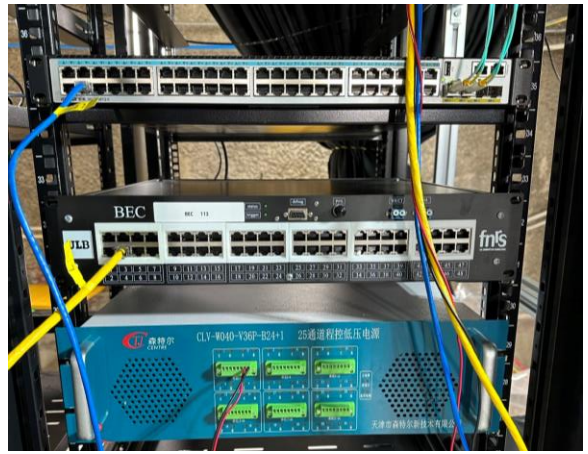
- Specification:
  - Provide full waveform digitization with high speed (1 Gsps) and high resolution (12-14 bits) ADC
  - Measure photon pulses with high resolution (full dynamic range: 1-4000 pe)
  - Global trigger and self-trigger support
  - Real-time charge and time calculation
  - System synchronization
  - Operate single PMT trigger at 50-100 kHz single trigger rate, and allow to stand high rates for very short times (up to 1 MHz for 1 s)
  - Safe remote reprogramming support
  - Over-voltage protection, independent channel power control
  - Power consumption: <10W/channel

Electronics structure





Under Water Box



Dry electronics in the electronics rooms

- DAQ switches,
- Back-End Card (BEC),
- Low voltage power supply(LV).

LPMT electronics group

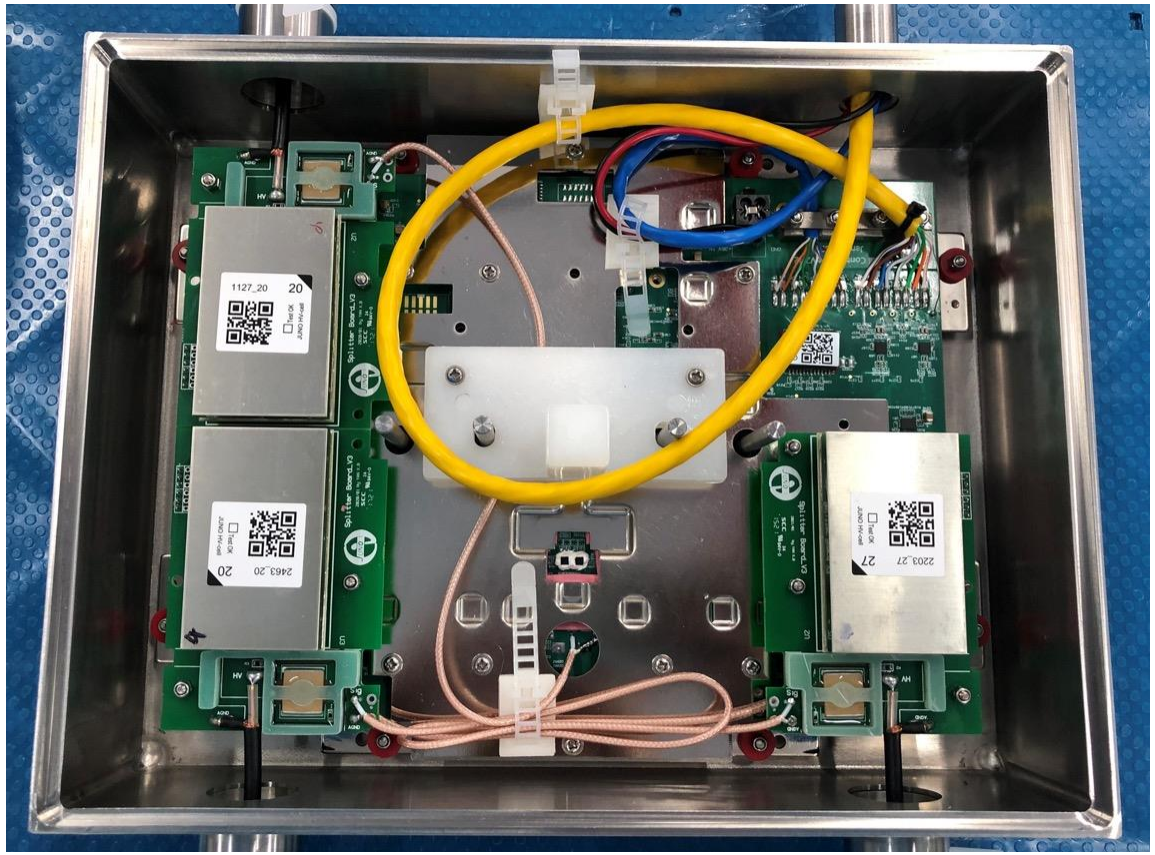
主要电子学部件	设计单位
核心ASIC器件	中科院高能所，清华大学
水下电子学盒	中科院高能所，意大利帕多瓦大学
高压模块	俄罗斯杜布纳研究所
水上电子学部分	清华大学，比利时布鲁塞尔自由大学

Electronics Manager：
- **江晓山 from IHEP，**
- **Alberto Garfagnini from University of Padova and INFN**

Under Water Box

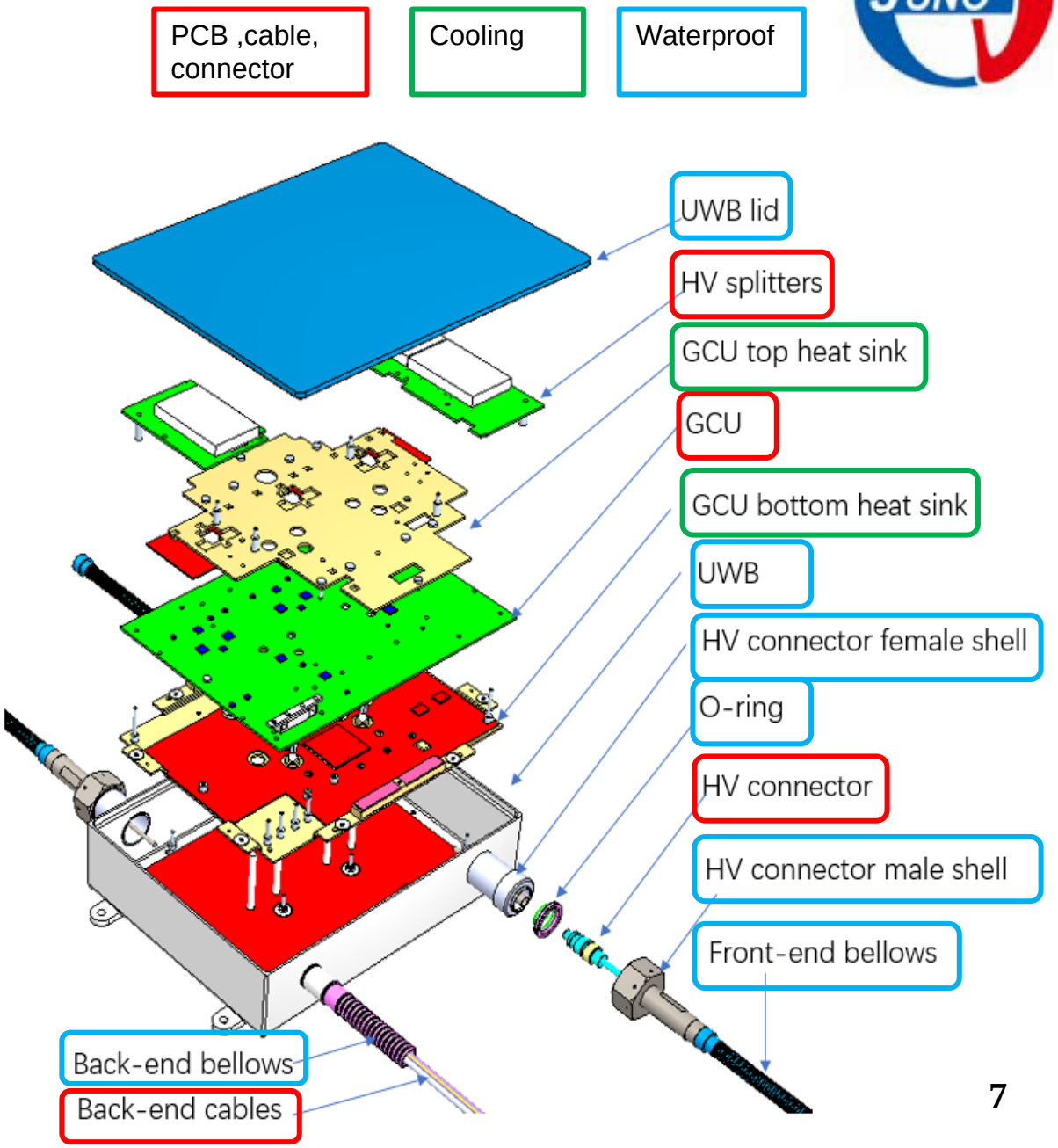
Bellow to PMT

Bellow to Dry electronics

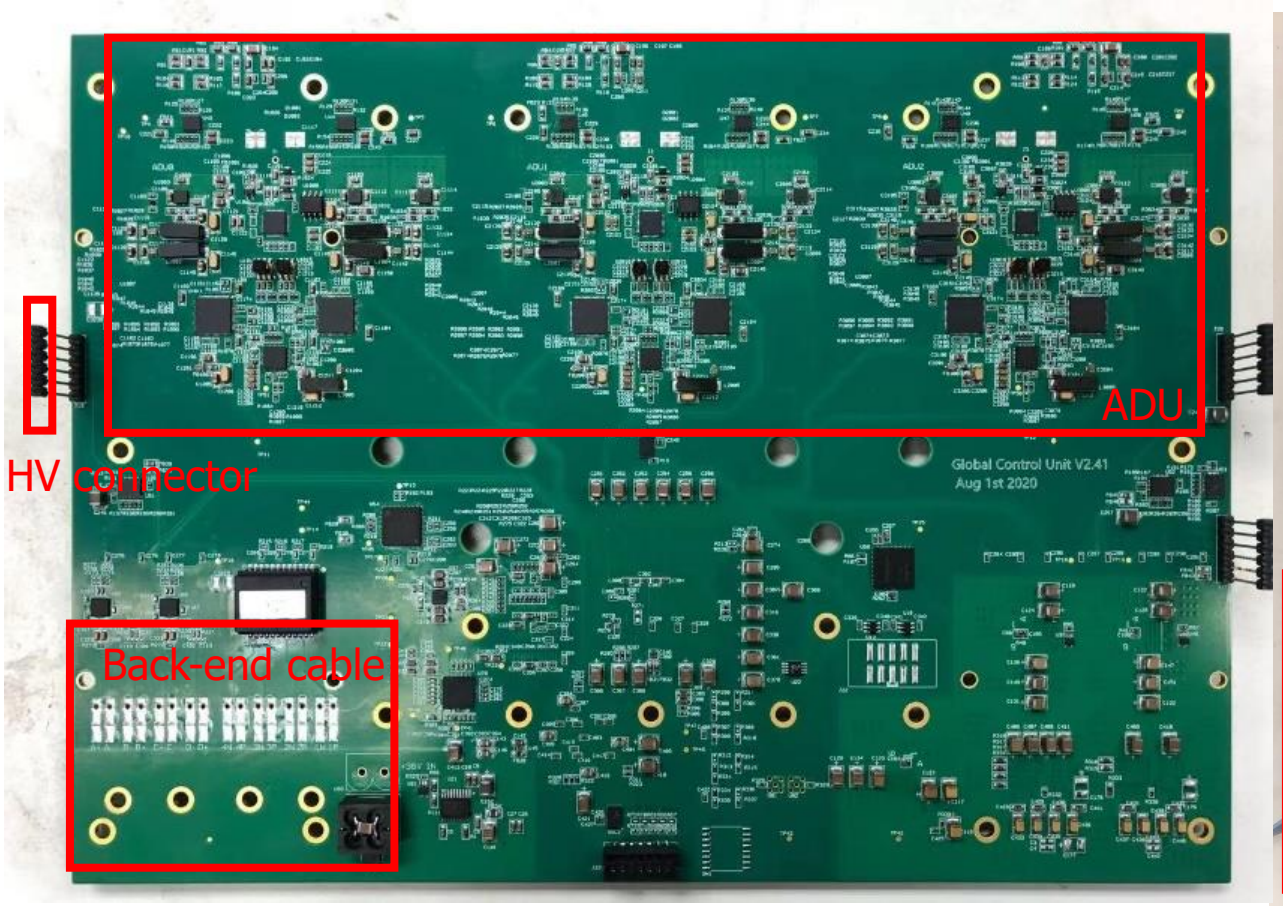


Bellow to PMT

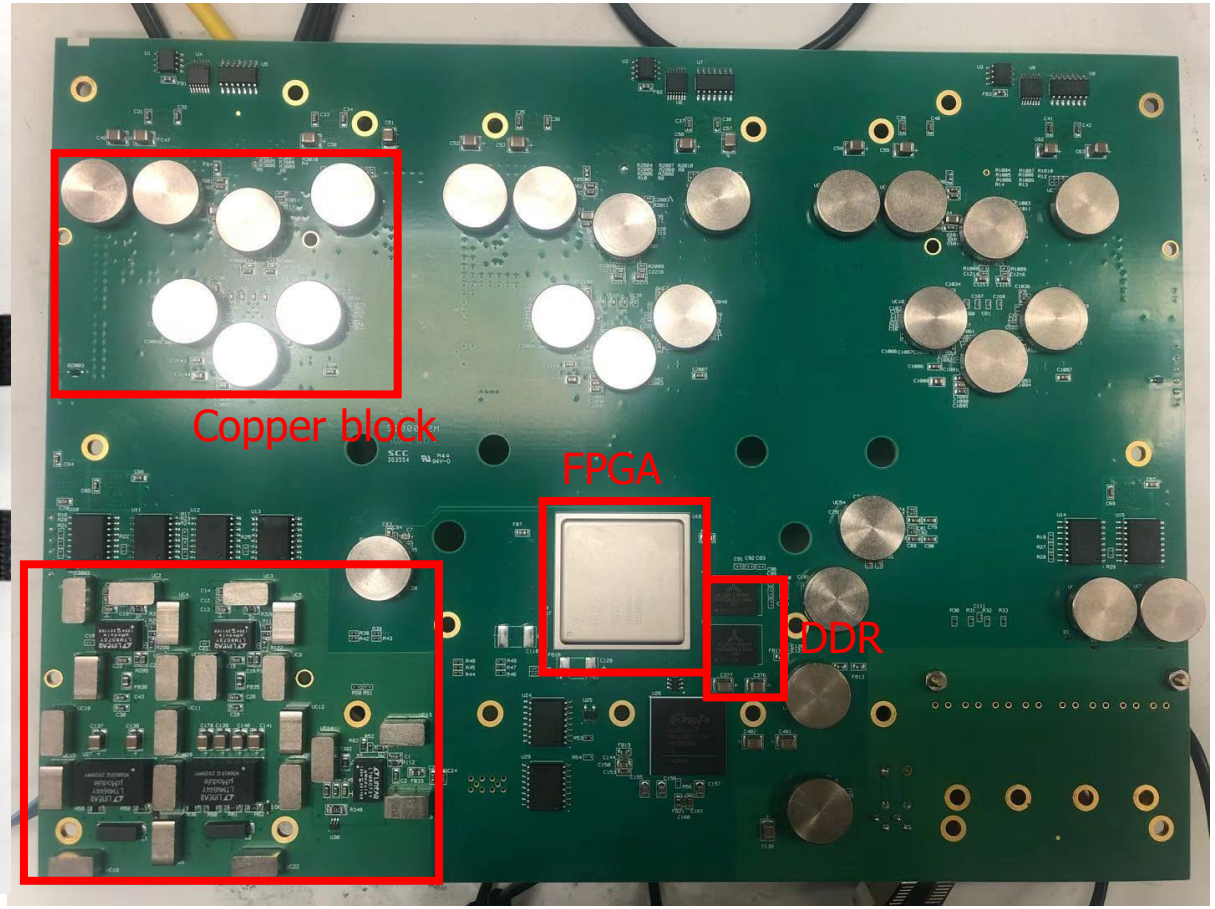
Bellow to PMT



Global Control Unit (GCU)

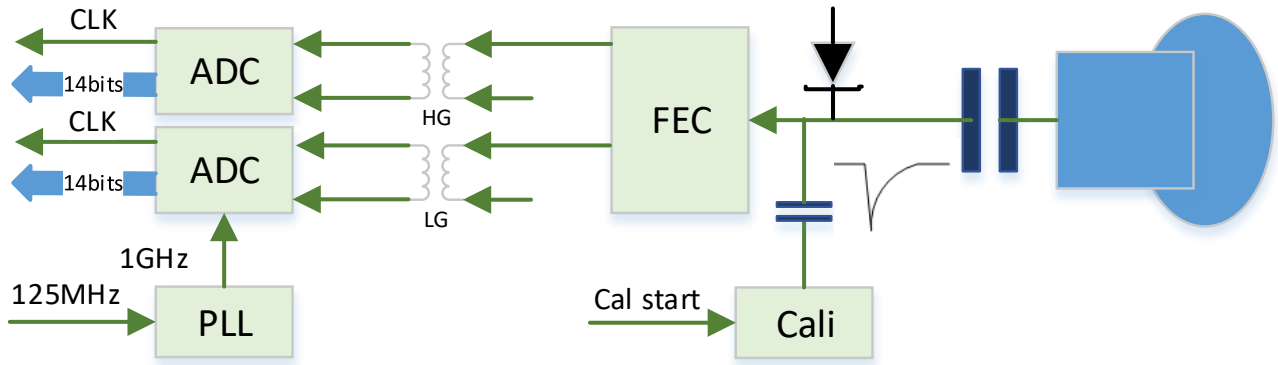


Component side

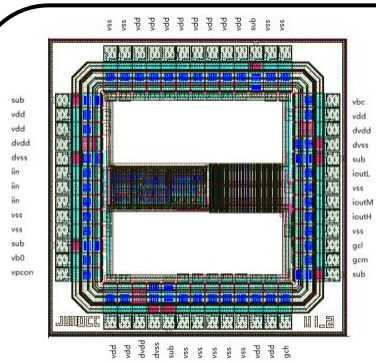


Cooling side

Analog-Digital Front-end Unit (ADU)



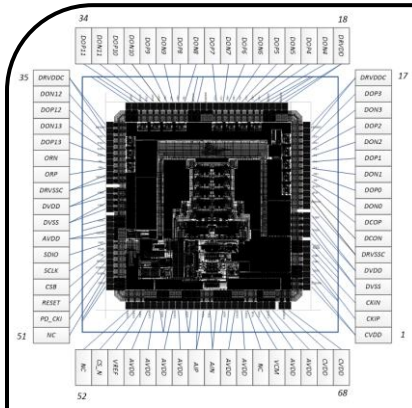
- Dynamic ranges:
  - Low Gain(8:1): 0~7.5V(4000pe)
  - High Gain(1:1): 0~960mV(128pe)
- Dual channels 1Gsps FADCs.
- Energy resolution: 0.1pe@1-100pe, 1%@>100pe
- Adjustable self-test pulse inject
- Over-voltage protection from circuit and FEC chips itself.



by 严雄波 from IHEP

FEC: A current amplifier ASIC

- Package：QFN40 (5mmX5mm)
- Consumption：100mW
- Range：1, 1/8
- Noise (RMS)：< 3.2uA (0.023pe)
- Input impedance：1.1 Ω@10MHz

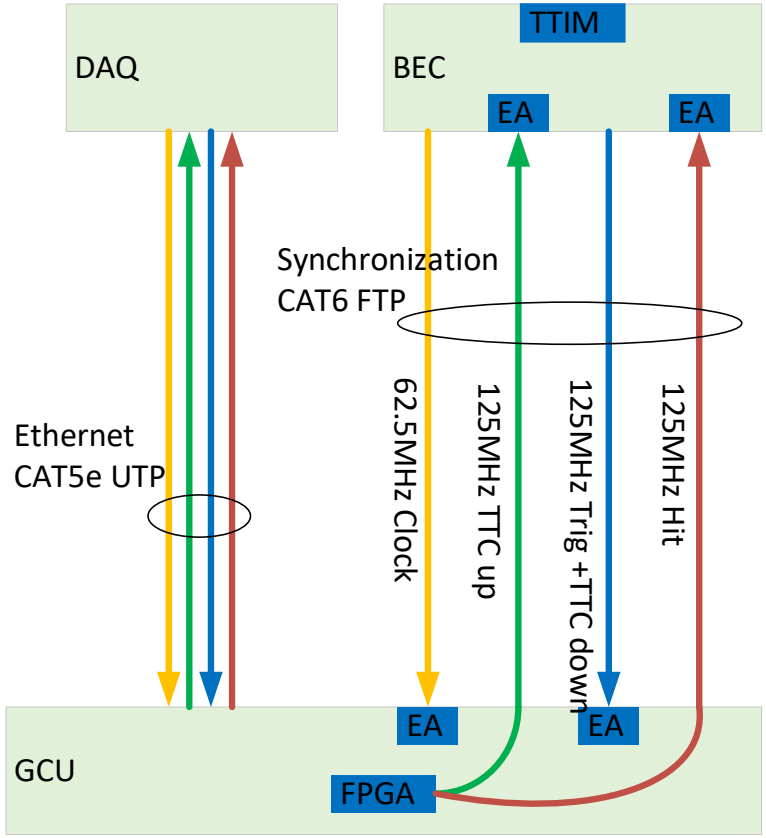


by Tsinghua

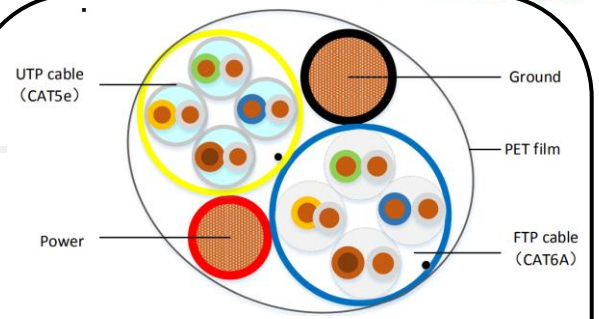
FADC:

- 12bit, 1GSPS
- ENOB of 10 @ fin up to 200MHz @ 1GSPS (-1.0 dBFS)
- SFDR = -68 dBc @ fin up to 200MHz @ 1GSPS (-1.0 dBFS)
- DNL < ±0.5 LSB, INL < ±2 LSB @12-bit level
- Power < 800mW

Back-end transmission



- CAT6 FTP for synchronization
  - FPGA drives signals to the cables
  - Cable Equalizer receives the signals from the cables
  - Synchronized 62.5MHz clock fan-out to GCUs
  - Real-time Hit information upload to TTIM
  - TTC protocol transmits real-time global trigger and 1588 protocol for clock alignment
- CAT5e UTP for Ethernet readout
  - IPBUS&TCP protocol on FPGA
  - RGMII interface to PHY

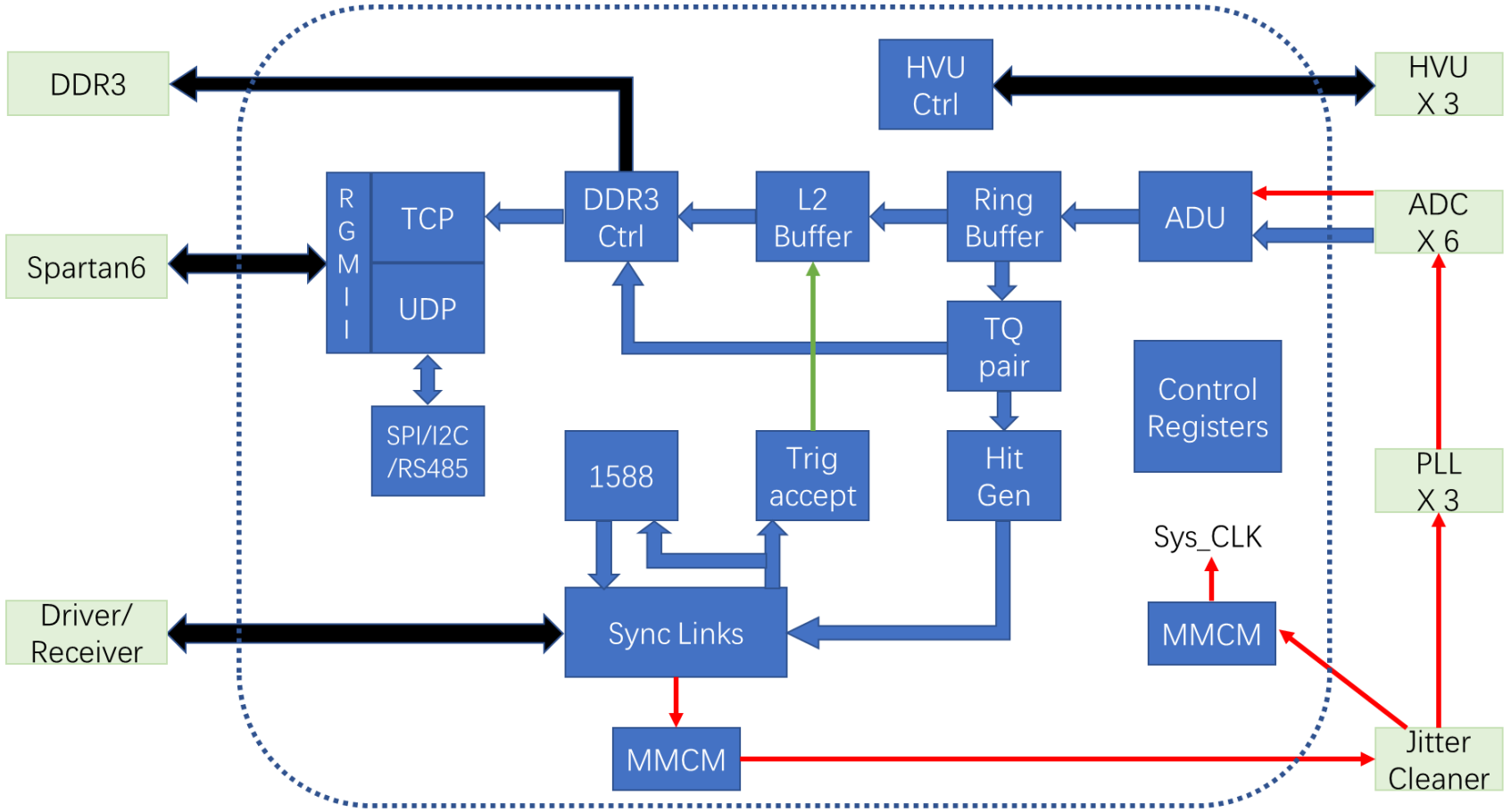


(by 孙芸华)

Cable pairs	BERs(60hours)	
1,2 (GCU1/2)	No loss of lock	No loss of lock
3,6 (BEC)	$<3.70X10^{-14}$	$<3.70X10^{-14}$
4,5 (GCU1/2)	$<3.70X10^{-14}$	$<3.70X10^{-14}$
7,8 (BEC)	$<3.70X10^{-14}$	$<3.70X10^{-14}$

PRBS test with 100m cables

FPGA firmware logical structure



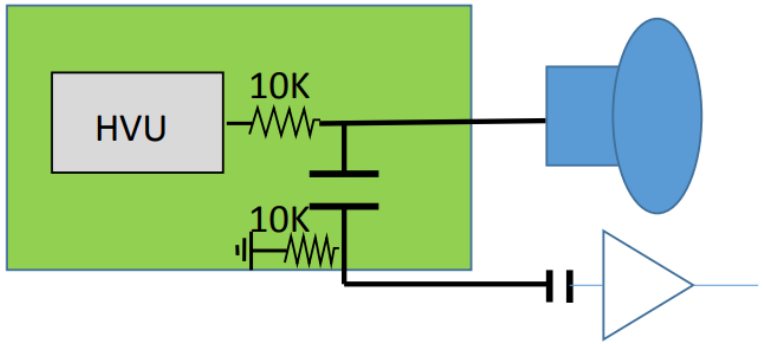
XC7K325T-2FFG900

Main function block

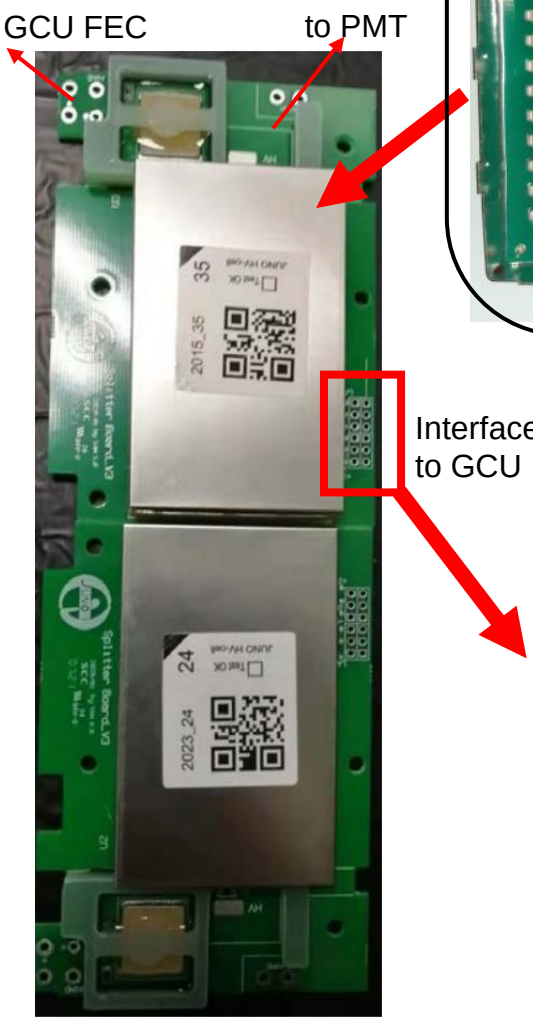
- Clock generator
- Analog to digital conversion unit (ADU)
- Storage management
- Data processing logic
- Synchronization link
- Ethernet protocol
- High voltage unit control
- Control and status registers

HV splitter

(by 严雄波)



- Function
  - Serve as a motherboard to the HVU and distribute the high voltage to the PMT,
  - Decouple the DC high voltage from the AC signal of interest for read-out.
- Requirement
  - Noise < 0.1pe
  - HV withstanding > 2000V

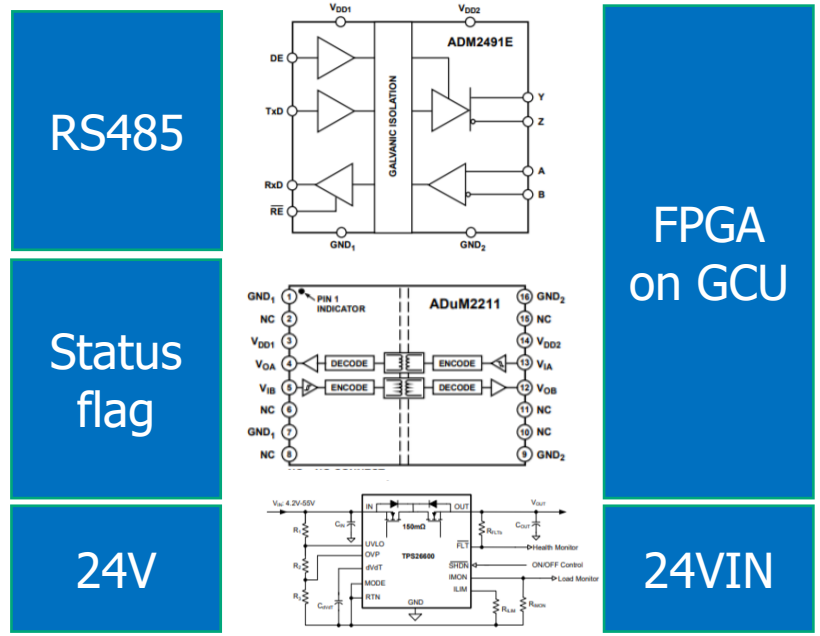


Splitter of 2 channels

HVU (by JINR)

High Voltage Unit (HVU)

- Range of HVU is 800V-3000V in steps of ~0.5V.
- Ripple: 10 mVpp
- HV long term stability: 0.05%
- Temperature coefficient: 100 ppm/◦C
- Maximum output current: 300 μA

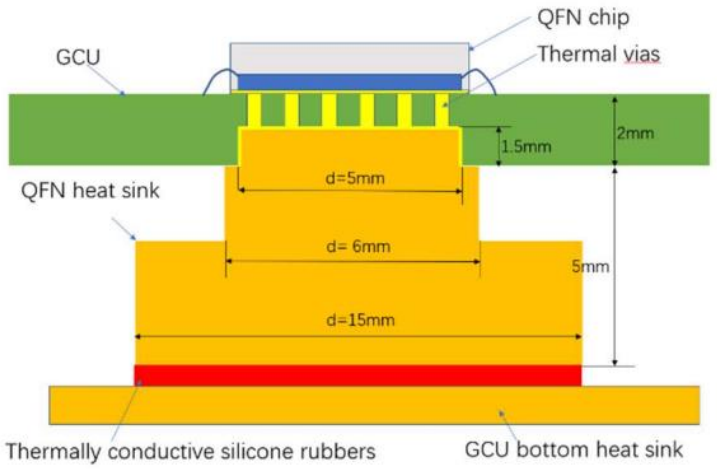


Isolator for HV signal and PW on GCU side

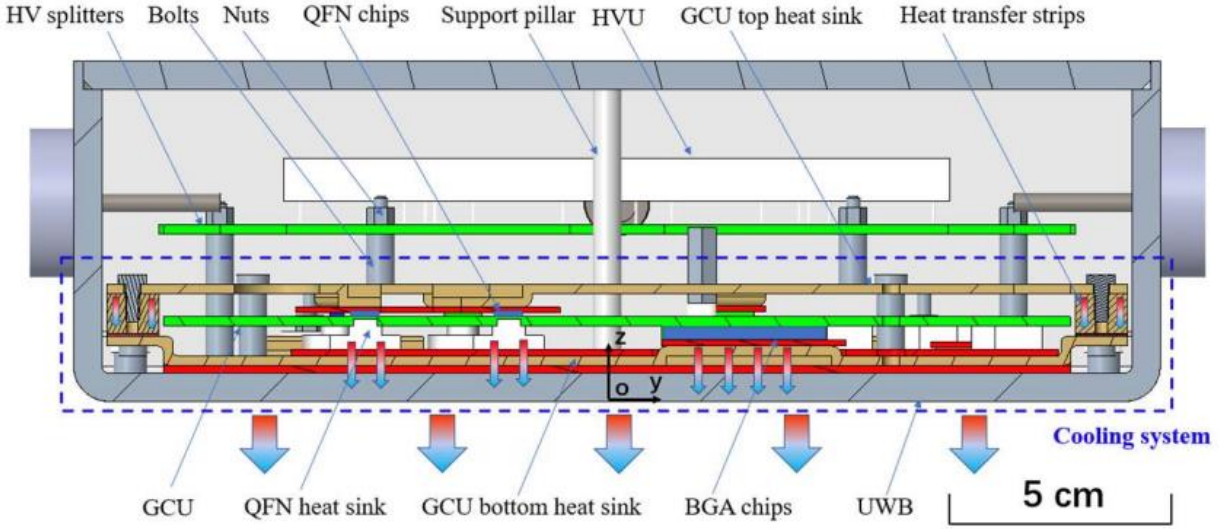
Cooling mechanical design

(by 王仰夫)

- Goals：Keep the case temperature of the component lower than 30℃ (under ~25W, ambient temp: 22℃)
- Features：
  - The bottom side of PCB serves as the primary heat transfer path.
  - BGA chips on the bottom side will transfer heat via the chips' top.
  - QFN chips on the top side will transfer heat via the copper block under the chips.
  - Additional copper blocks are placed close to DC-DC to aid in heat dissipation.



Copper block under QFN chips

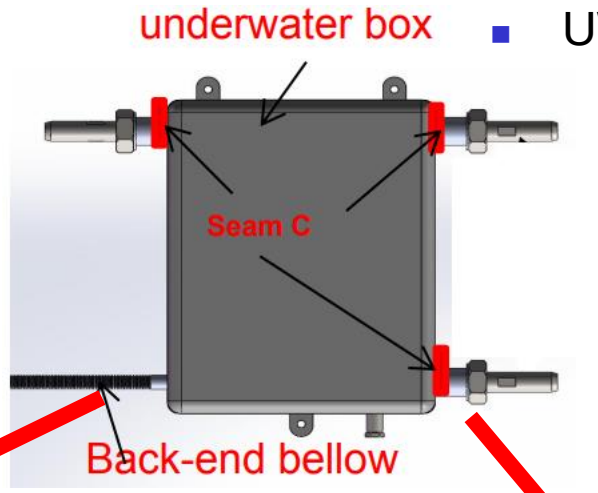


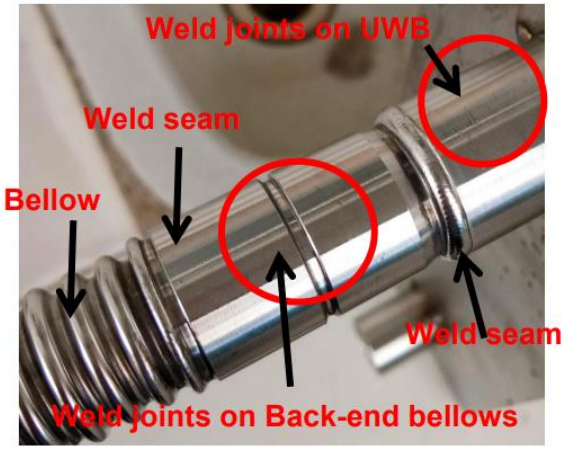
Structure inside the underwater box

Waterproof design

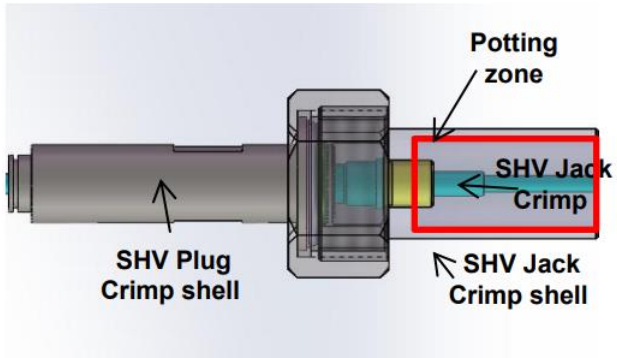
(by 王仰夫)

- UWB with a 60m-90m backend bellow by argon arc welding.





- UWB and its lid sealing by laser welding
- UWB with 3 HV connector female shell by argon arc welding.



- HV connector shell sealing by 3 O-rings.

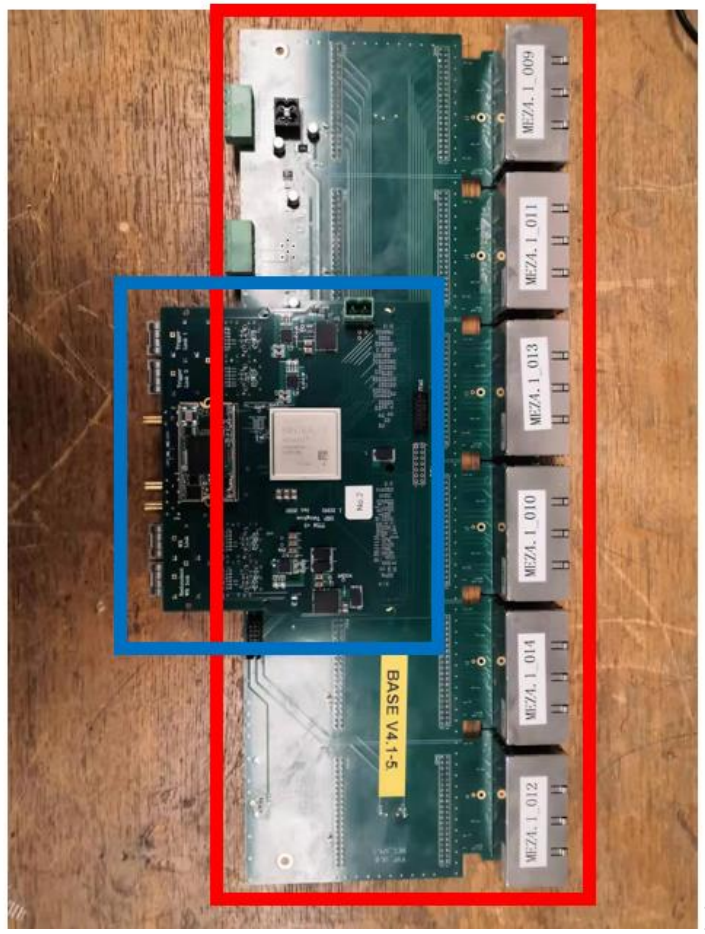
underwater box with long bellows

Back-End Card (BEC)

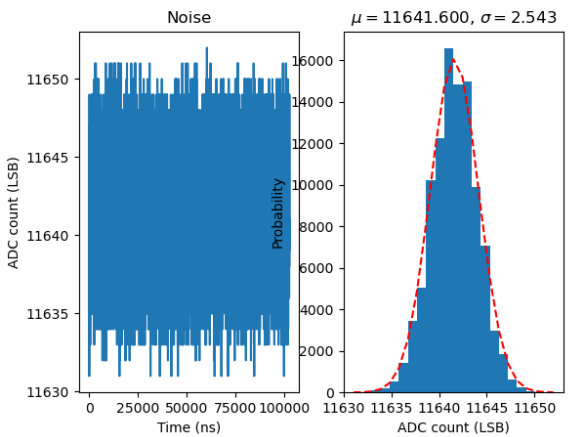
- The Back-end Card makes the connections between the GCUs and the trigger electronics via CAT6 cables.

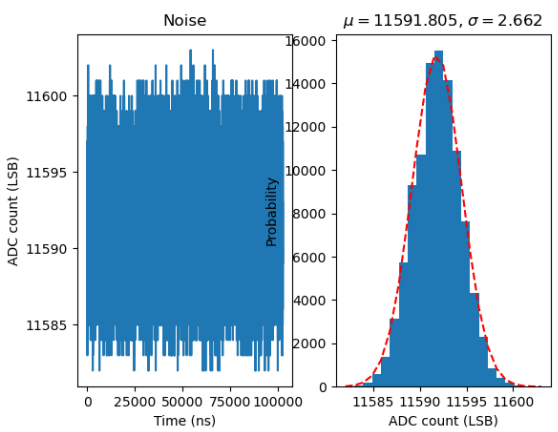
- Red box: Base board receives 48 Ethernet cables from underwater boxes. (by 杨一帆 from ULB)
- Blue box: Trigger/Timing interface mezzanine (TTIM) distributes the CLK signal to GCUs and transfers the TRG signal between Global Trigger and GCUs. (by 董建蒙from Tsinghua)

- Synchronous link: fixed latency link. Timing and trigger control (TTC) protocol. Nominal link speed 125 Mbps.

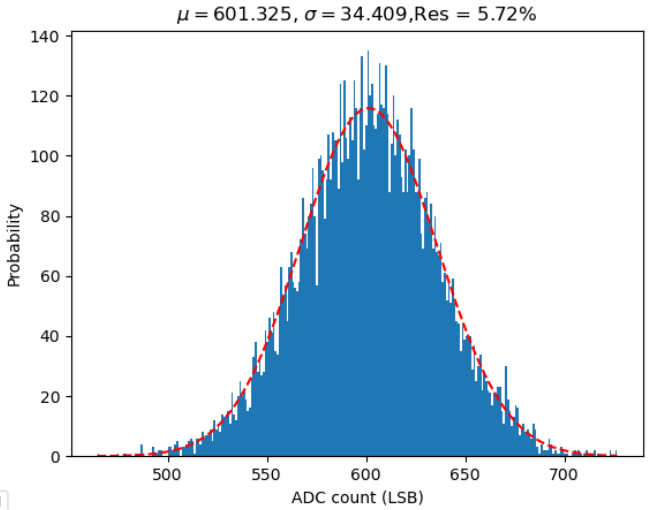


Front-end performance



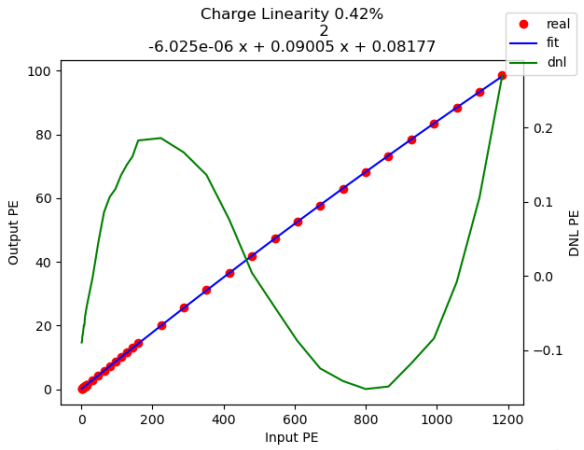


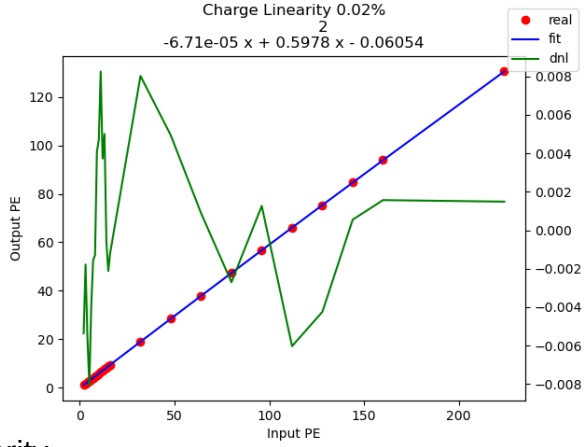
Noise



Energy Resolution

- Electronics test with self-test pulse
  - Noise: < 400uV HG (SPE:7.5mV)
  - Linearity: < 0.5% HG
  - Energy Resolution: < 10%

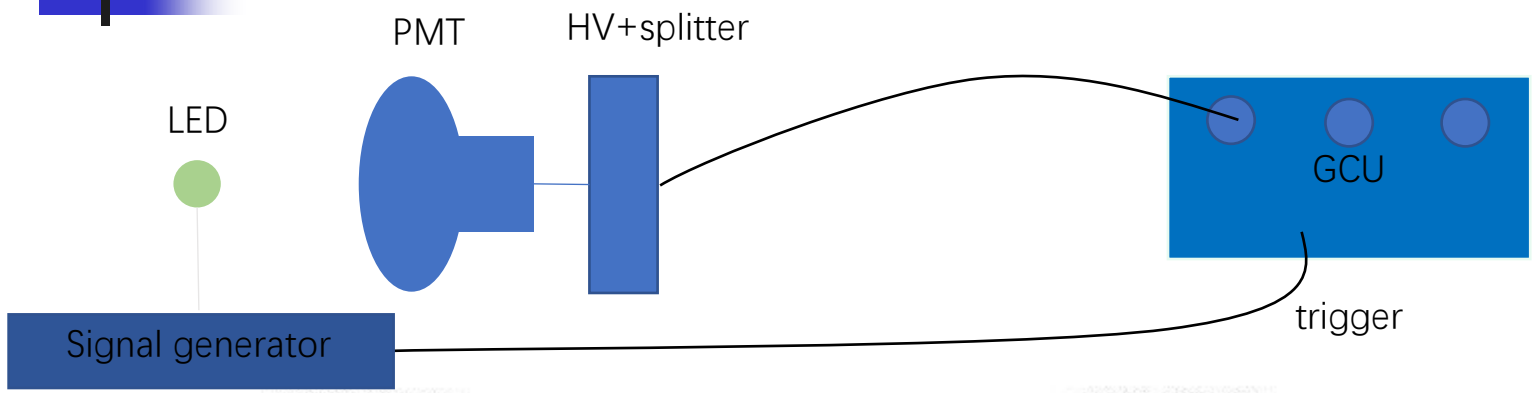


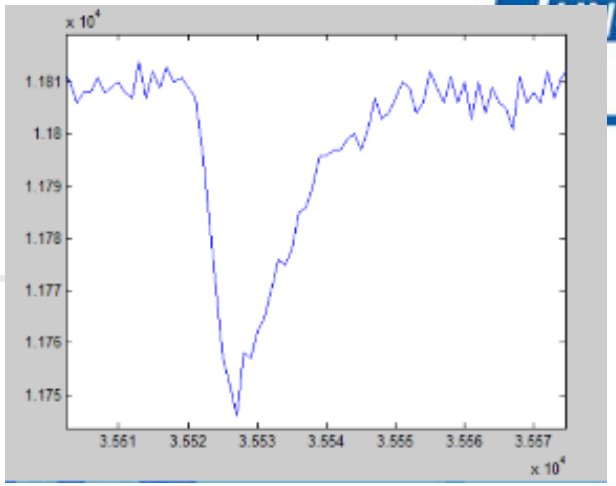


Linearity

	CH1 LG	CH1 HG	CH2 LG	CH2 HG	CH3 LG	CH3 HG
Gain	0.079	0.54	0.078	0.54	0.078	0.53
Input noise (mV)	2.54	0.39	2.66	0.39	2.28	0.37
Linearity (%)	1.27	0.43	1.09	0.32	1.24	0.29
Energy Res (%)	0.38@ 100pe	6.81@ ~1pe	0.35@ 100pe	5.77@ ~1pe	0.4@ 100pe	5.76@ ~1pe

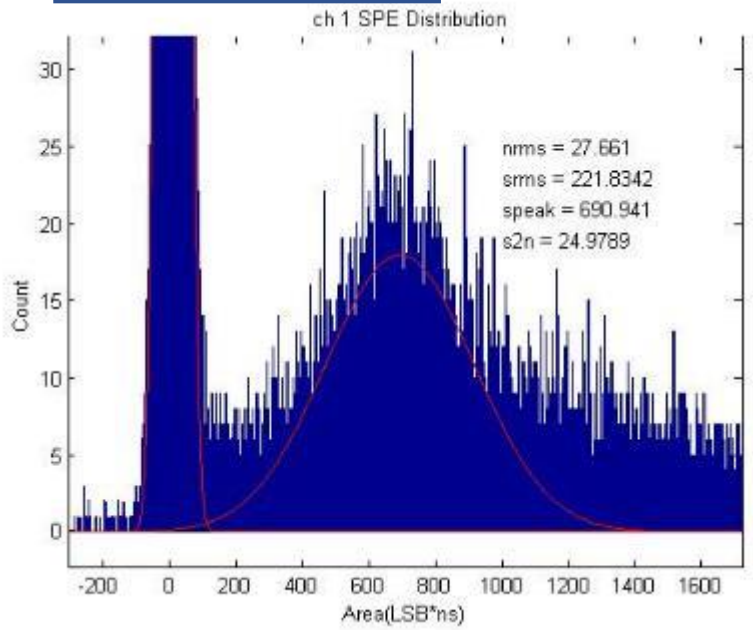
SPE distribution test

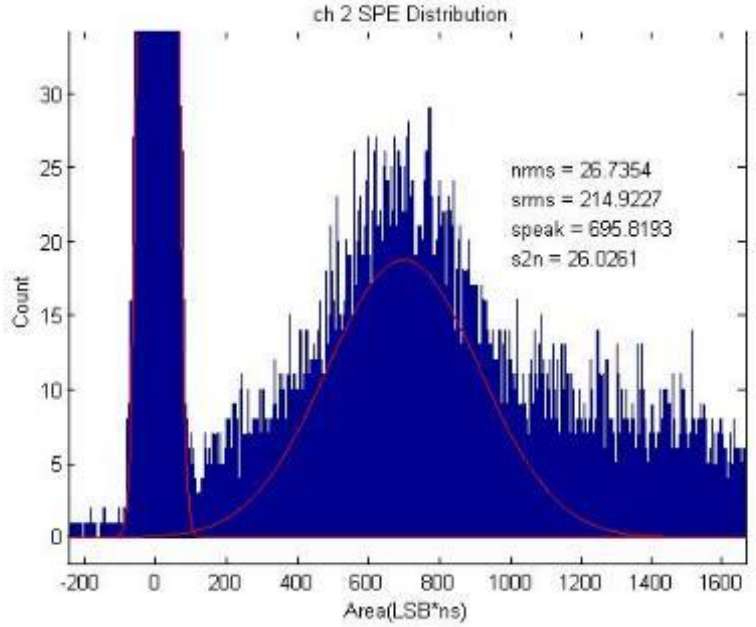


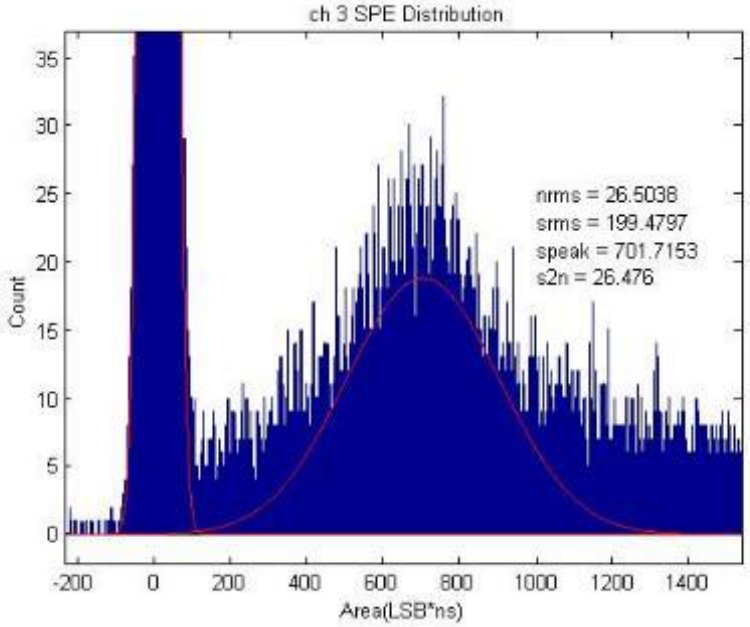


Typical spe waveform(LPMT)
~ 70 ADC LSB

Signal to Noise rate > 20

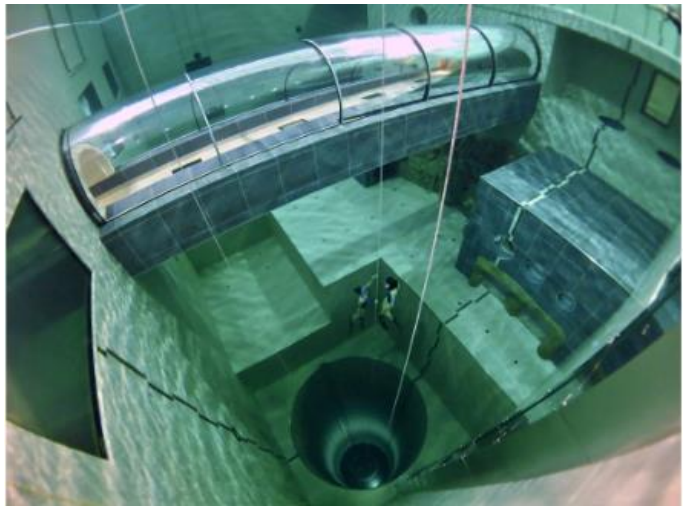




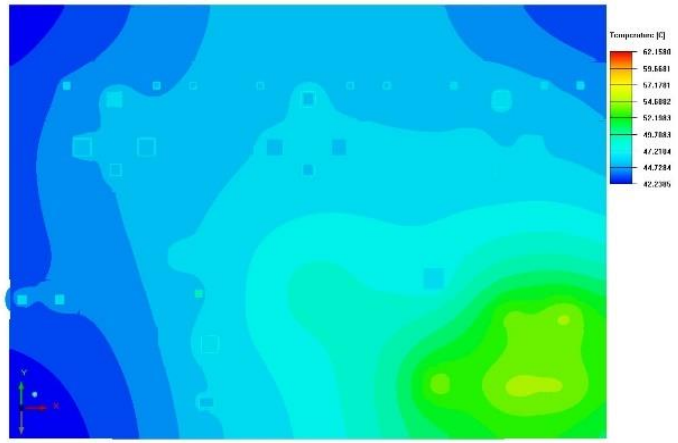


Cooling test

Water tank in IHEP



40m swimming pool in Italy



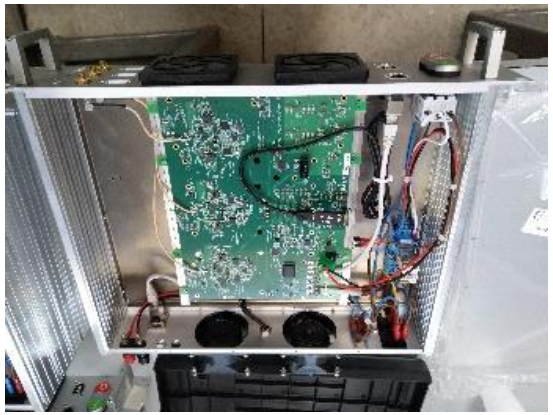
GCU temp. distribution (CFD simulation)

Tca(case-to-ambient)	DC-DC	Jitter cleaner	ADC	FEC	LDO
In 19.2℃ air	28.6	26.6	26.5	26.6	26.9
in 20.5℃ water	6.0	6.9	6.4	5.9	5.9

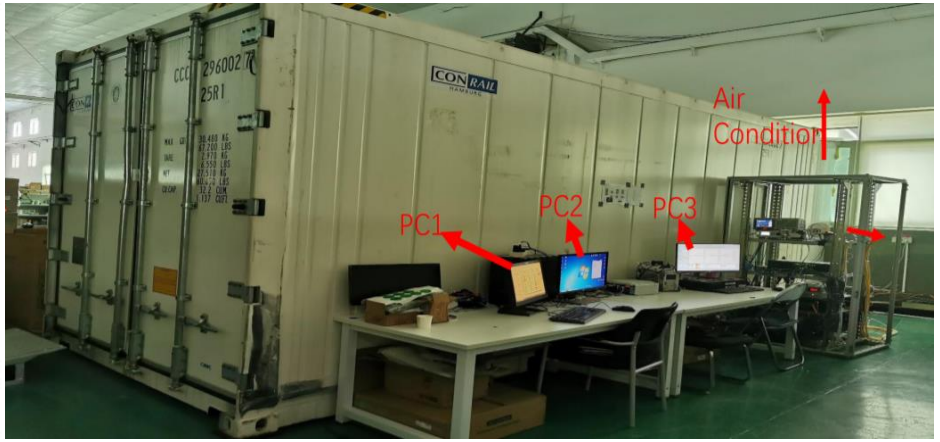
All chips are **less than 30 ℃** in 20.5℃ water

Integration Test

IHEP, Beijing

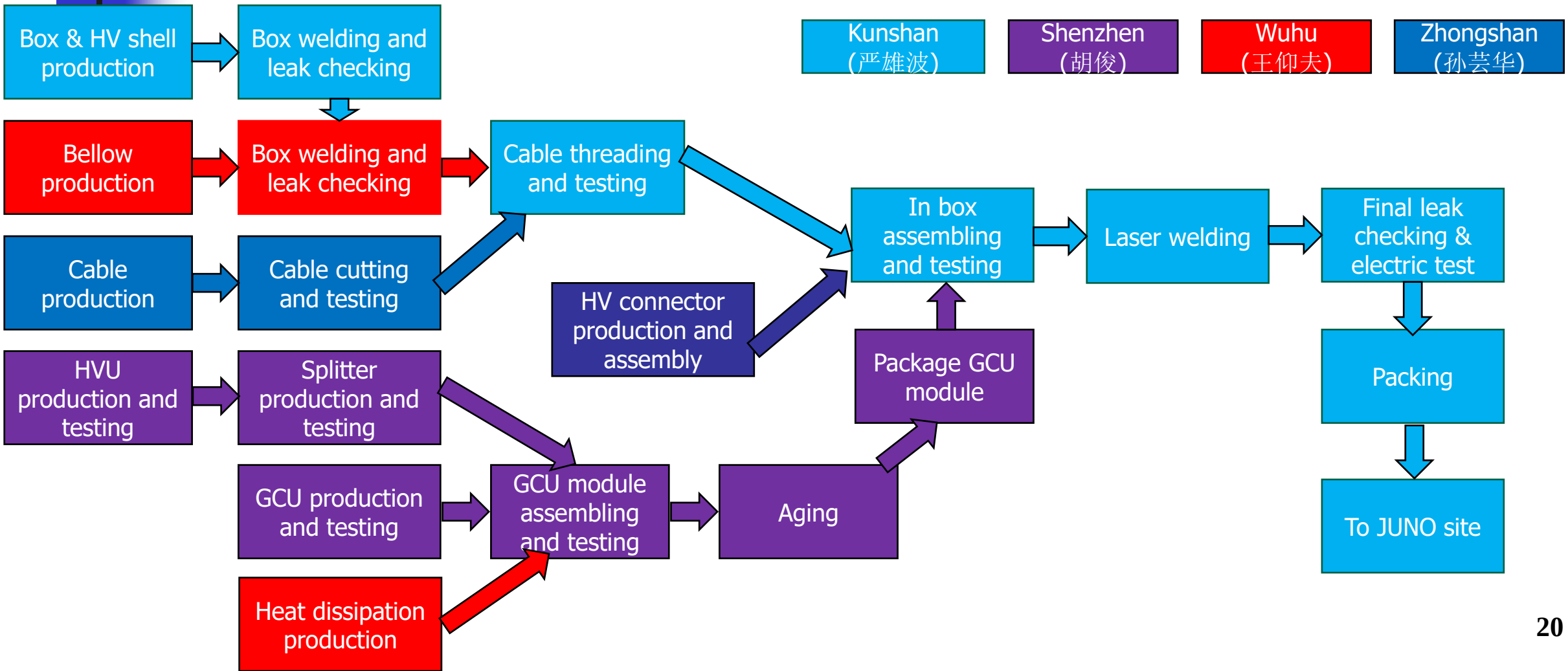


Padova, Italy



Zhongshan

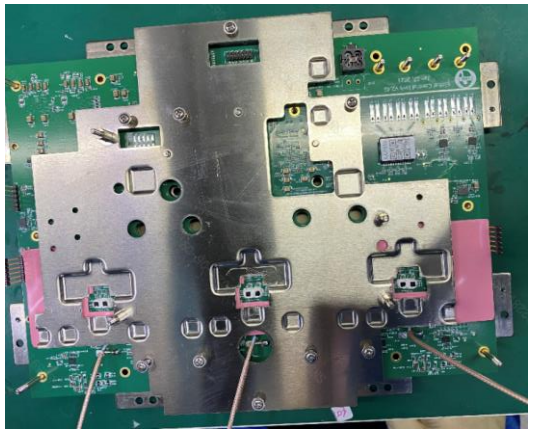
UWB production (2021.1-2022.10)



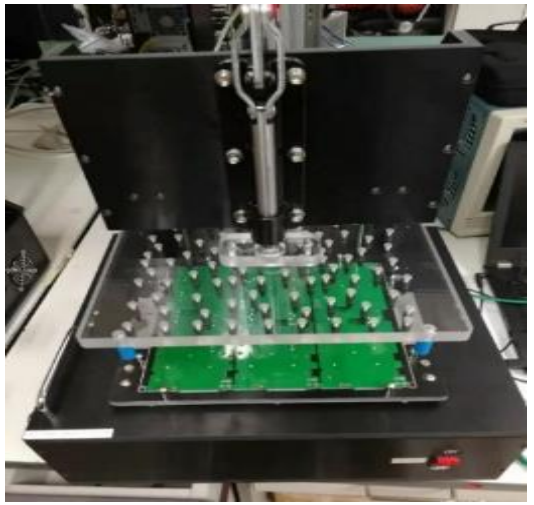
Production in Shenzhen

GCU & splitter board

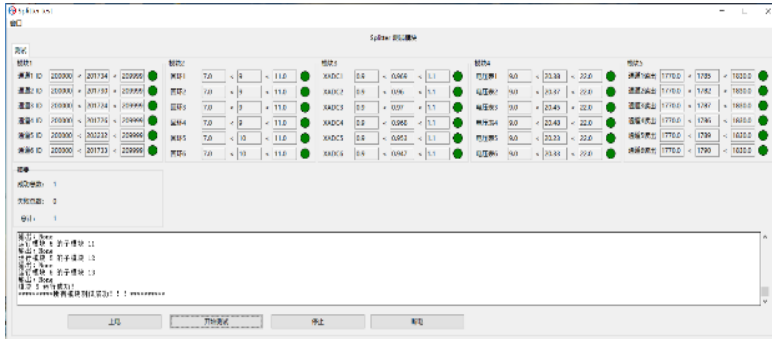
flatness check of the heat sink



GCU module after assembly



Electrical testing fixture

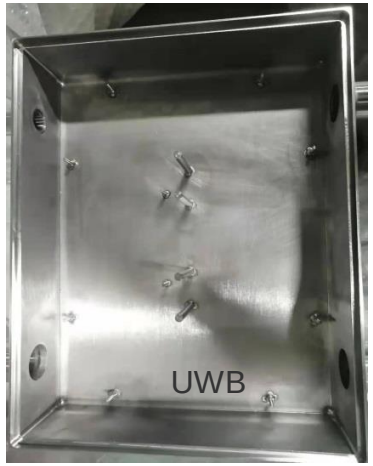


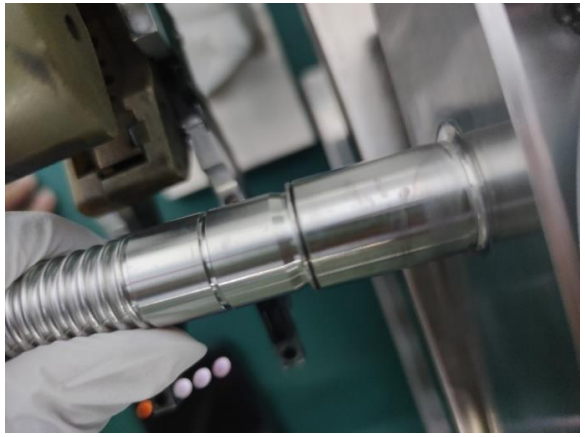
Test software GUI

Aging test

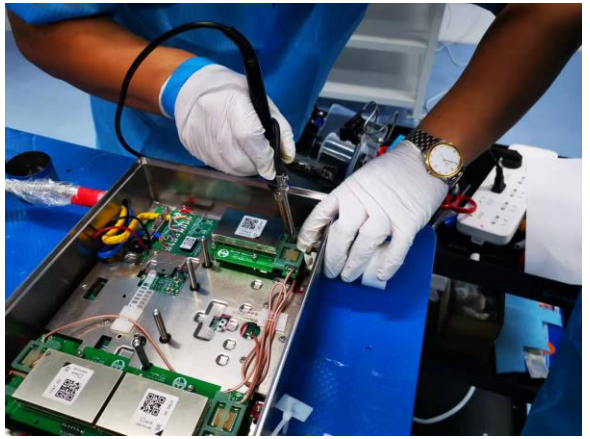
Package for transportation

Production in Kunshan





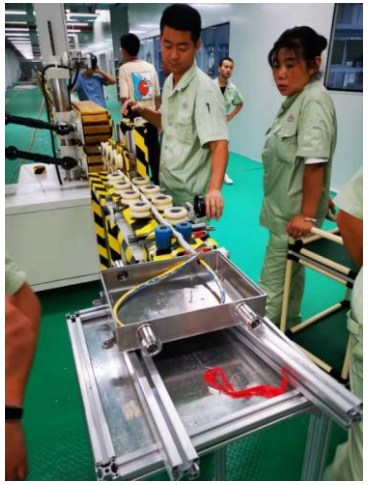
Argon-arc welding



Assembly in box

Long term test

Leak check



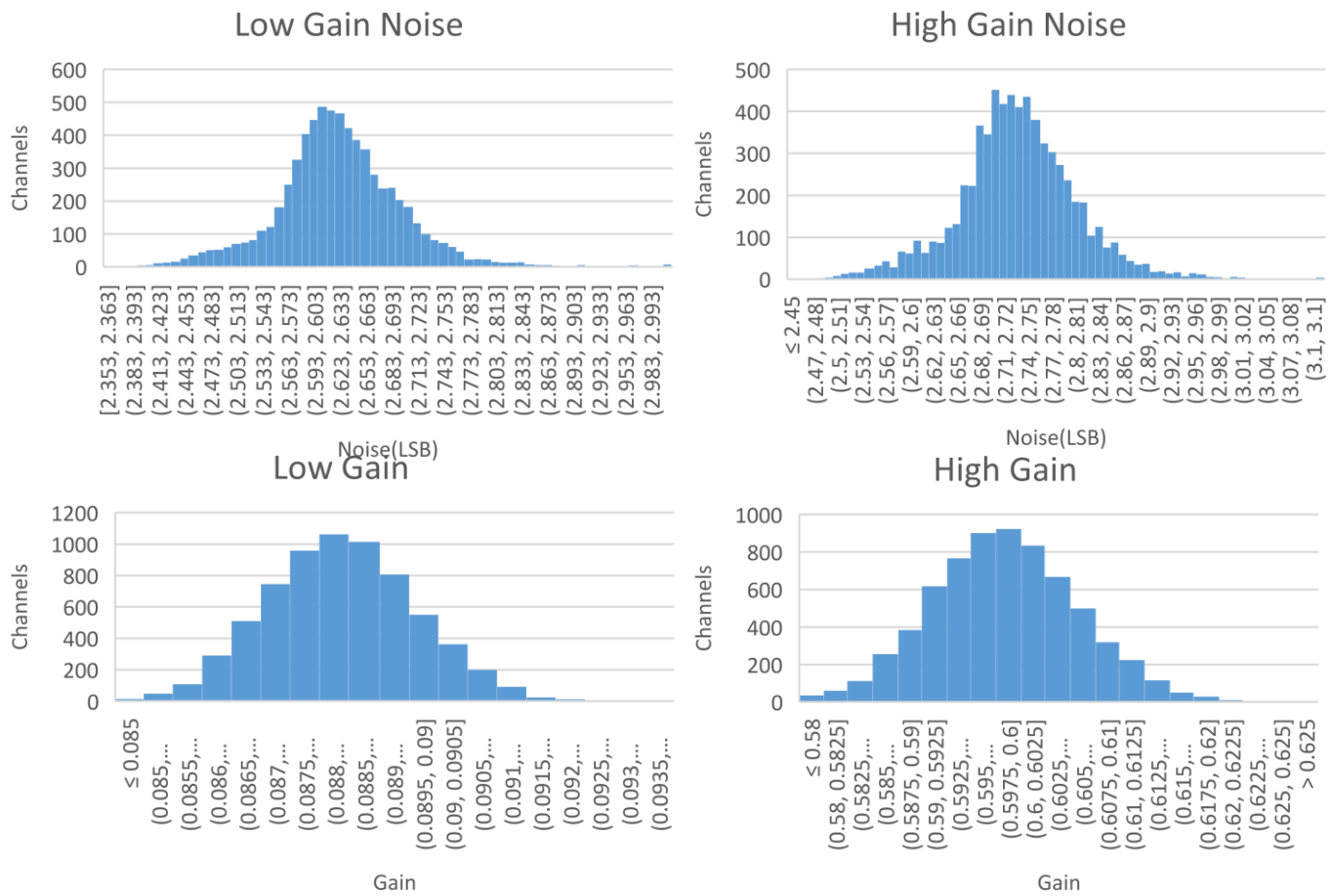
Cable threading

Laser welding

Electrical testing fixture

Package to JUNO

Production summary



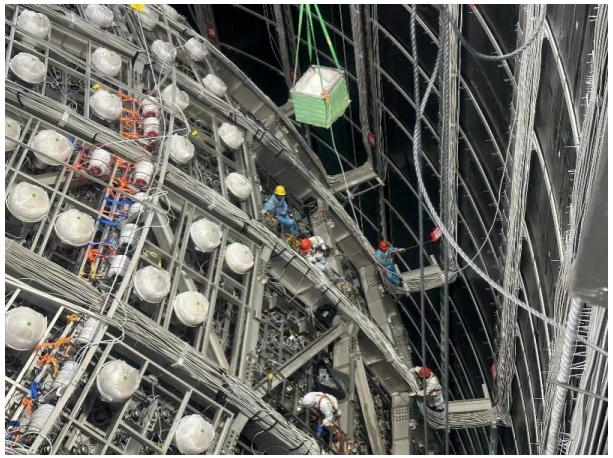
- Shenzhen produces 6950 GCU modules at a yield rate of **99.22%**
- Kunshan produces 6883 UWBs at a yield rate of **98.27%**
- We require **6681** UWBs on the SS, with ~**3%** spare, including OSIRIS, prototypes, etc.

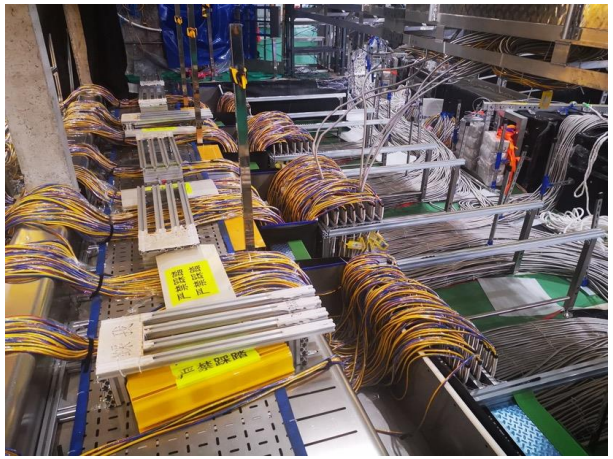
Installation on JUNO site

LPMT Electronics installation

(supervised by 樊磊)

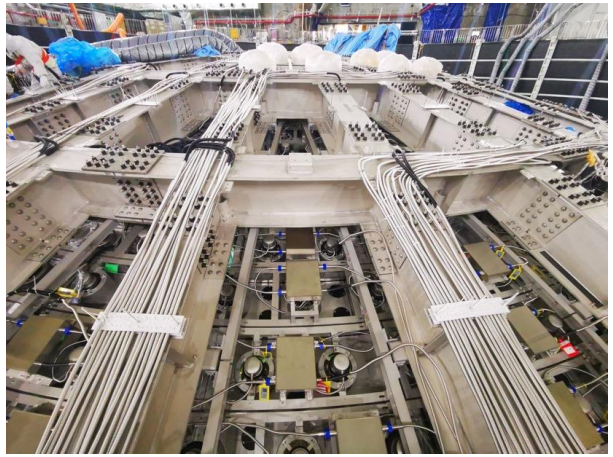
Transportation to underground



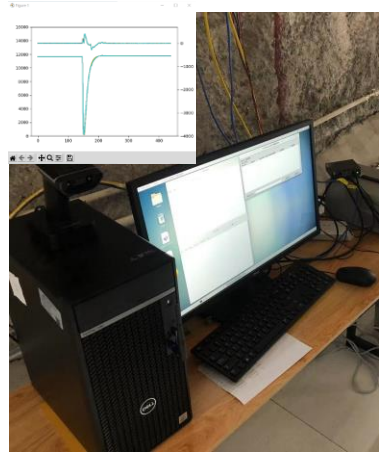


Nitrogen room

Connected to racks in Electronics room



Installation on the steal structure

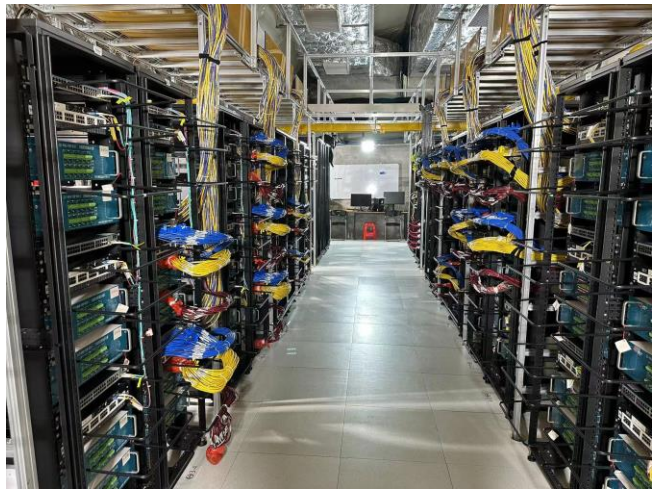


Leak check and refection test

2074(CD)+
177(VETO)
LPMT UWBs
were installed.
(~30%)

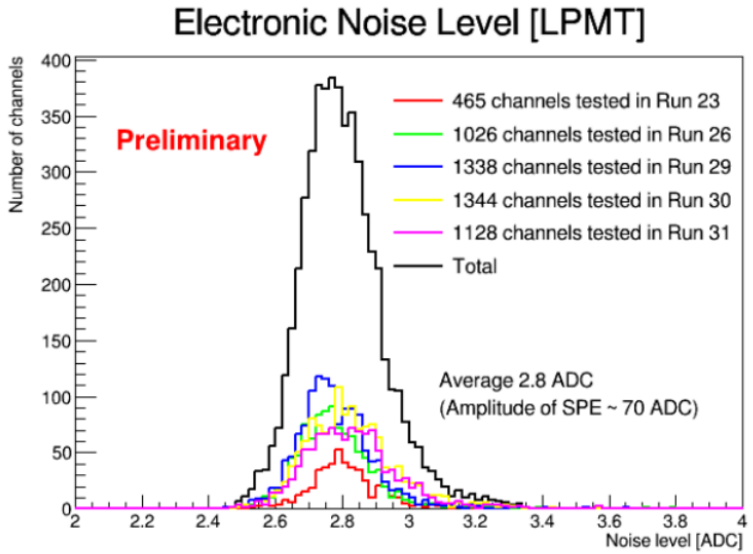
Commissioning test

(by 于泽源)



Electronics room after installation

Light off test

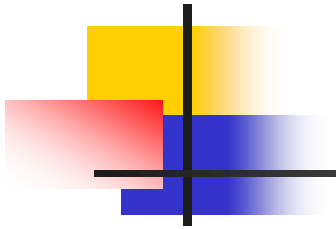


Electronics noise

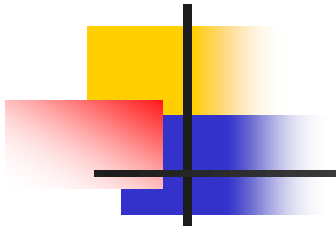
- **RMS of baseline: 4% of SPE amplitude**
- **RMS of integration: ~2.5% of SPE integral**

Summary

- Due to JUNO high scientific objectives, the LPMT readout electronics have stringent requirement, including a large number of channels, high resolution, high reliability.
- The production of the electronics components has been completed with a high yield rate.
- The installation is currently in progress.
- Premilitary tests demonstrate the high performance of electronics.

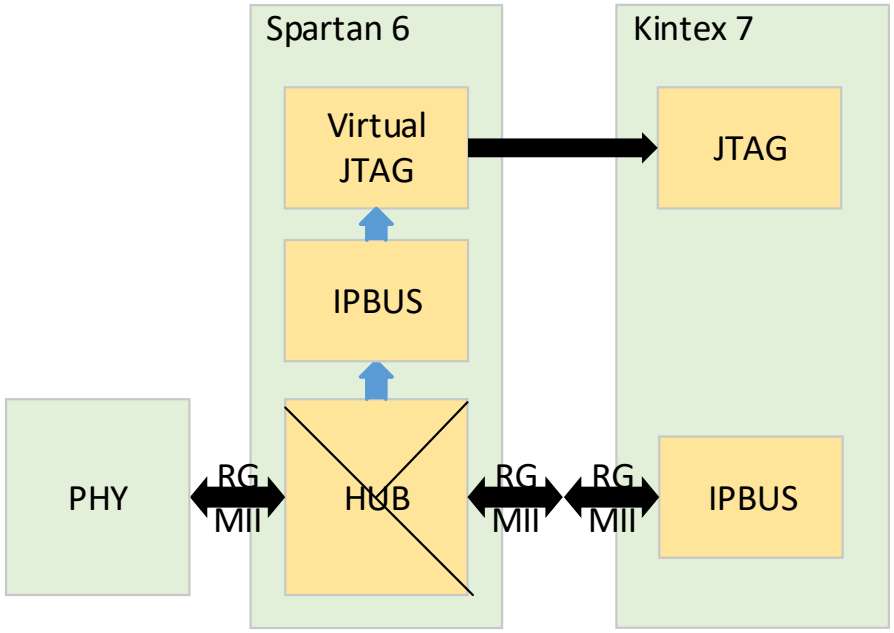


Thank you for your attention!



BACK UP

Remote Reprogramming Support



- Dedicated Spartan 6 FPGA for remote update firmware
- Implement a 2-port Ethernet hub in Spartan 6.
  - Main data path is connected to K7 port.
  - JTAG reconfiguration data is connected to S6 port.
- Implement the RGMII interface between PHY chip and S6, also between S6 and K7.
- The Ethernet communication between PC and GCU is successful.

System Reliability Estimation

	FIT	30℃	35℃	40℃	
affect 1 channel	HV + Splitter Board	23.5@2kV + 0.21	38@2kV + 0.21	57@2kV + 0.21	Sum is F_front
	ADU	14	22.7	34	
affect 3 channel	Front Bellows	0.5	0.5	0.5	Sum is F_back
	Connector (double Viton O-ring)	<12.1x3	<12.1x3	<12.1x3	
	GCU	76.4	88.5	100	
	Back Bellows	0.5	0.5	0.5	
	Electronics box	1	1	1	

Temperature [℃]	F_front	F_back	Failure channels in 6 years
30	>38	>115	>180
35	>61	>127	>210
40	>91	>138	>250

Note: 2 pieces of DDR are not included