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Development of low-temperature low-noise low-background HPGe CMOS front-end electronics

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A cryogenic low-noise CMOS preamplifier has been successfully developed for HPGe detectors for the CDEX dark matter search experiments. The noise of the ASIC was optimized for 1pF input capacitance. The prototype chip was implemented in GF 180 nm CMOS process and was fully evaluated at low temperature. The power-on-reset module of the 2023 version of the preamplifier was tested. The rise time of the preamplifier was 48 ns when directly driving 1 meter long cable. The ENC was obtained to be 3.0 electrons for 0 pF input capacitances at 12 μs shaping time at 77 K.

Collaboration (if any)

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