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Development of cryogenic ASICs for HPGe detectors for dark matter and neutrino experiments

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Two cryogenic ASICs for HPGe detectors fabricated in 180 nm CMOS process for dark matter and neutrino experiments have been developed. One of them is a wide dynamic range CMOS preamplifier for neutrinoless double beta decay, and the other is a low noise CMOS preamplifier for dark matter detection. The wide dynamic range preamplifier consists of two-stage amplifiers. The first stage is a normal charge sensitive preamplifier and the second stage has dual gain channels to achieve large dynamic range up to 5 MeV. The ENC of high gain stage is simulated to be 4.9 electrons with 0.1 pA leakage current and 2 pF detector capacitance in 77 K, while the ENC of low gain stage is simulated to be 6.2 electrons. The low noise preamplifier is a normal charge sensitive preamplifier optimized for 2 pF detector capacitance. The ENC of the low noise preamplifier is simulated to be 4.5 electrons with 0.1 pA leakage current in 77 K. The chips have been submitted in May and will be received in September. Detailed circuit design and simulation results will be present in the talk.

Collaboration you are representing

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