Readout Electronics on Waveform Digitization and High-precision Time Measurement

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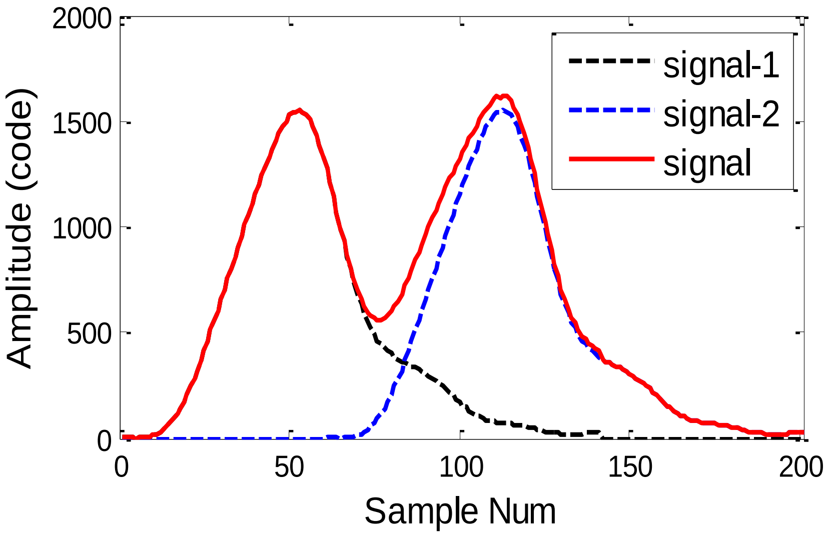
26/08/2025

Outline

- Introduction
- Waveform Digitization based on Time-Interleaved ADC
- Waveform Digitization based on Switched Capacitor Array
- High-precision TDC based Time Measurement
- Summary

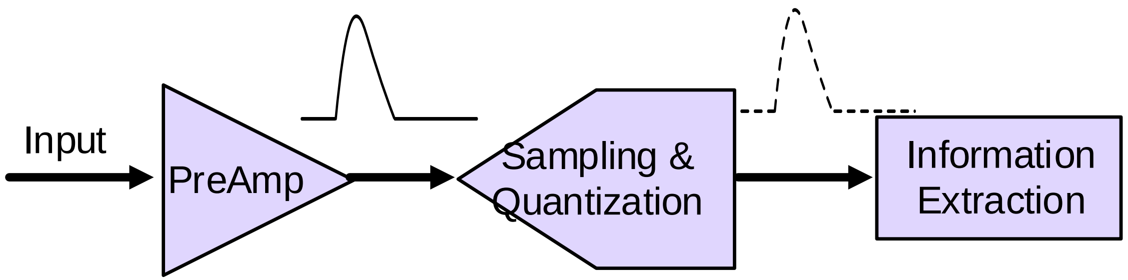
Introduction

- The basic information need to be measured in particle physics experiments
  - Charge, time, shape, count, etc.



- The classical charge & time measurement methods
  - Charge measurement: shaping and peak detection, ToT
  - Time measurement: discrimination + TDC
  - Each measurement needs a dedicated circuit

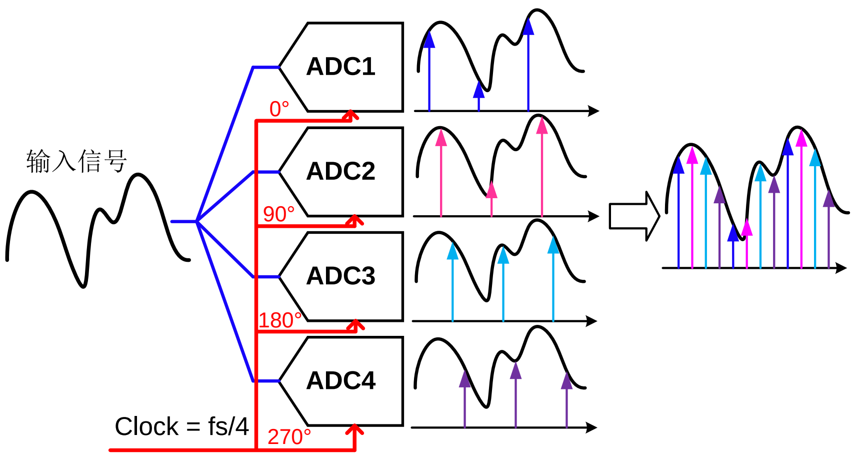
- Waveform Digitization
  - Raw waveforms from detector carry the most comprehensive information
  - Flexible algorithms can be used in the digital signal processing to get interested information
  - To be proven to have higher precision, especially in time measurement



Waveform Digitization Techniques

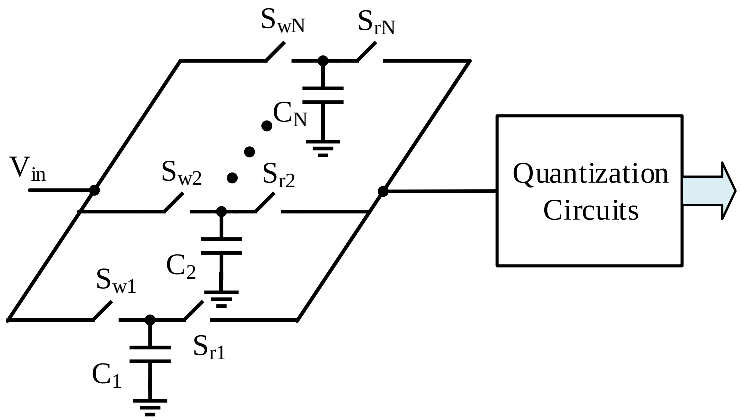
FADC

- High-speed sampling & high-speed quantization
- Small latency, no dead time, high resolution
- TIADC technique to boost sample speed
- High power consumption



SCA

- Switched Capacitor Array
- High-speed sampling & low-speed quantization
- Low power consumption and high channel density
- Work in trigger mode



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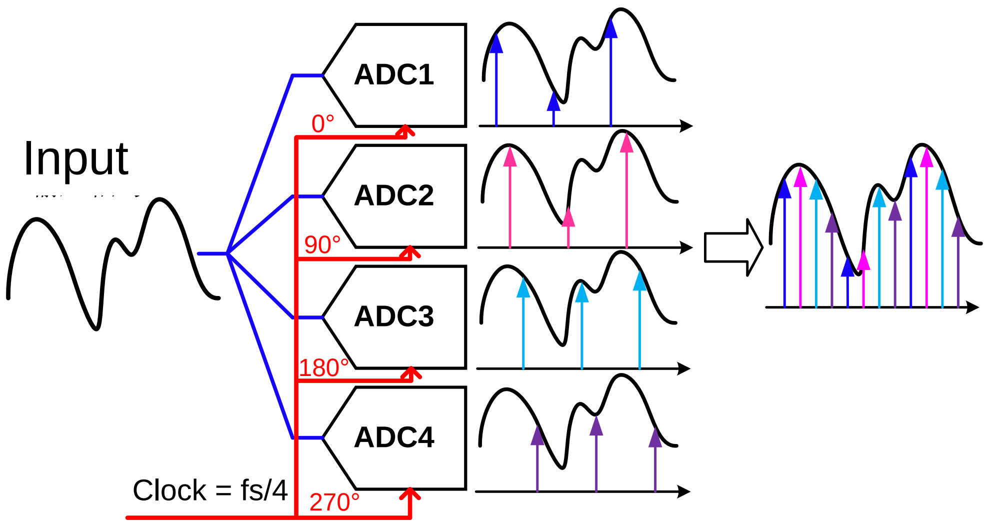
TIADC

- Time-Interleaved ADC
  - M parallel ADCs with sampling rate of Fs → M·Fs
  - Sampling phase if shifted by a fixed interval
  - Multiply the sampling rate and break through the sampling speed limitations of a single ADC

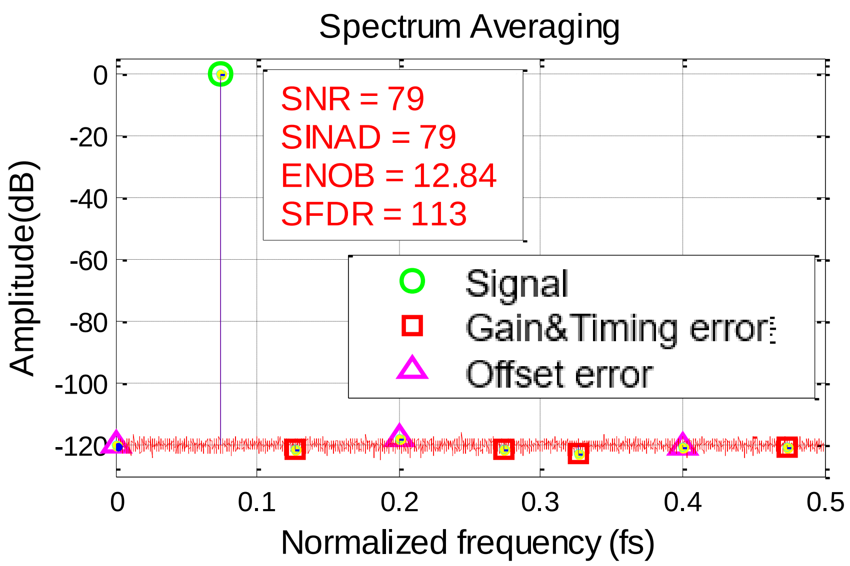


- Mismatch errors in TIADC
  - Offset Error: the difference between ground values
  - Gain Error: the difference between amplitude gains, from analog input to digital output
  - Phase Error: the difference between the sampling intervals of every two consecutive channel ADCs

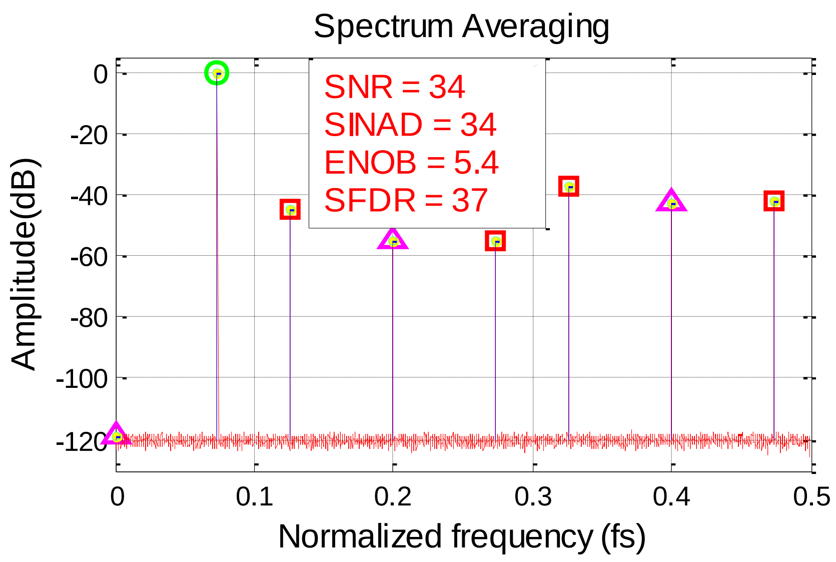
Mismatch errors deteriorate the system performance and limit its applicability.

Mismatch Error

The influence of mismatch error on the system spectrum



Without Mismatch

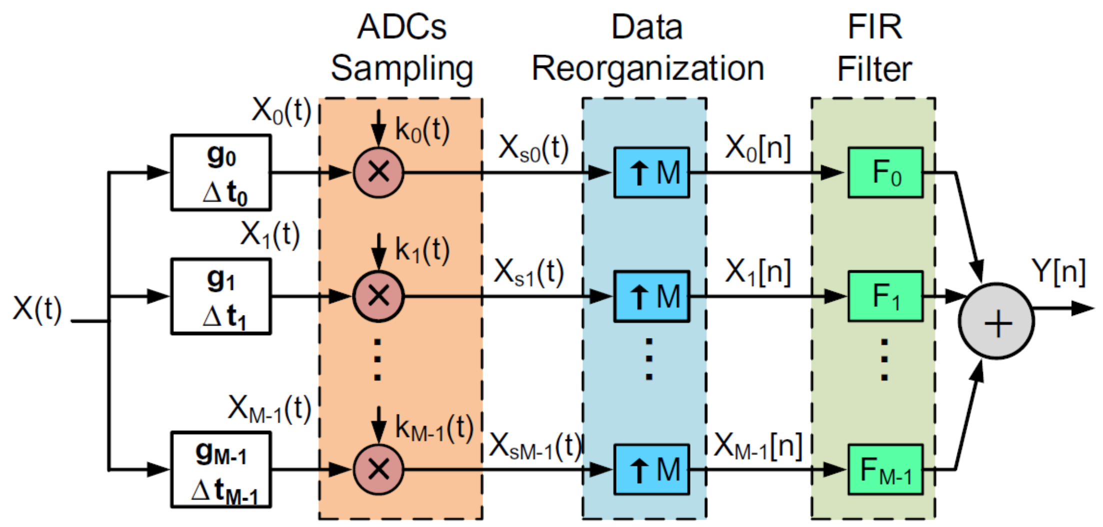


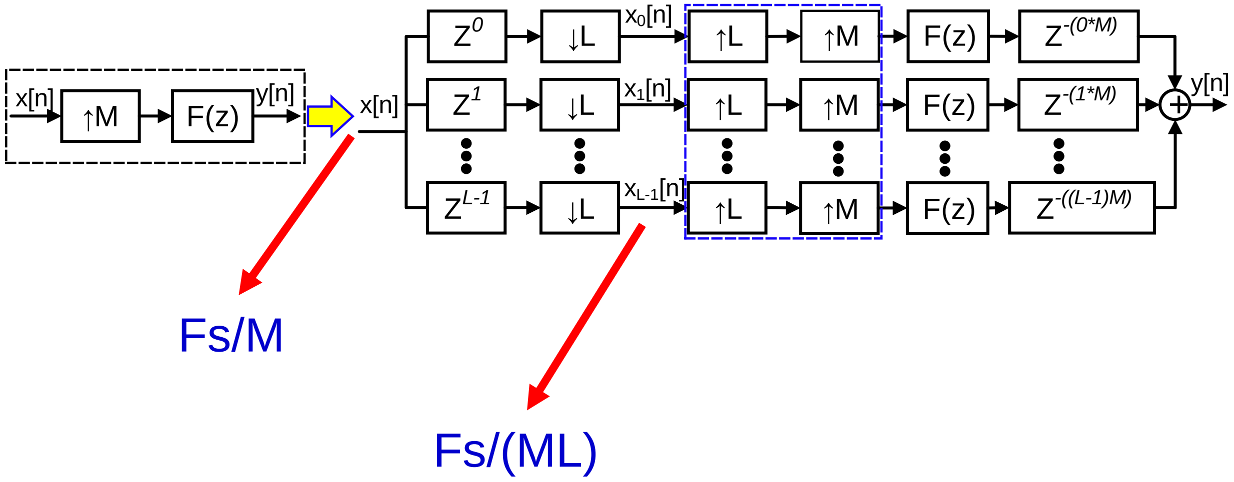
With Mismatch

- For narrow band signals, mismatch errors shrink to constants, easier to be corrected
- For wide band signals, **mismatch errors vary with input frequency,** making the correction complex

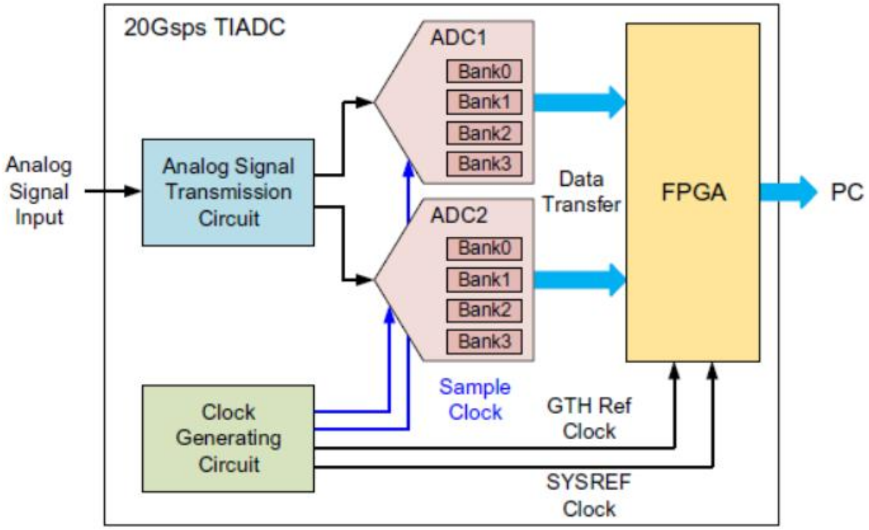
Mismatch Error Correction

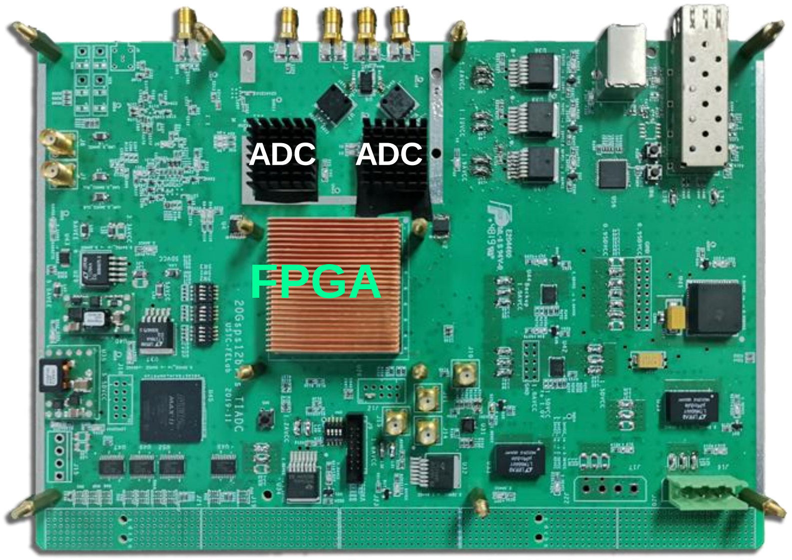
- The Perfect Reconstruction Filter can be approximated using FIR filter in the hardware
  - Each sampling channel has a FIR filter
- FIR implementation
  - Sampling rate of the ADC is much higher than the maximum operating frequency of an FPGA
  - Parallelization should be carried out to reduce the requirement for operating frequency

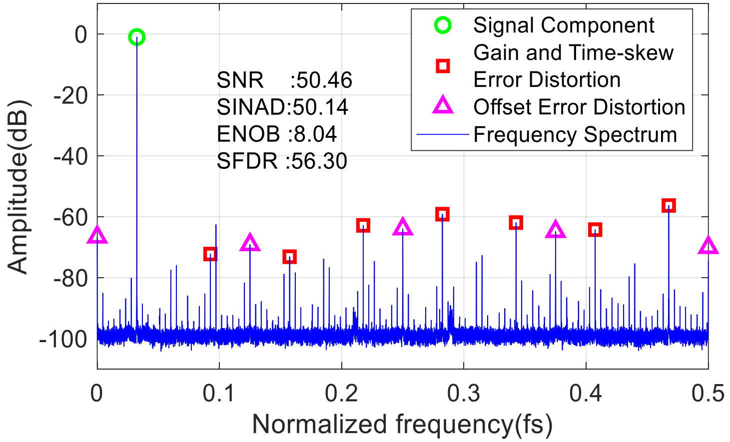




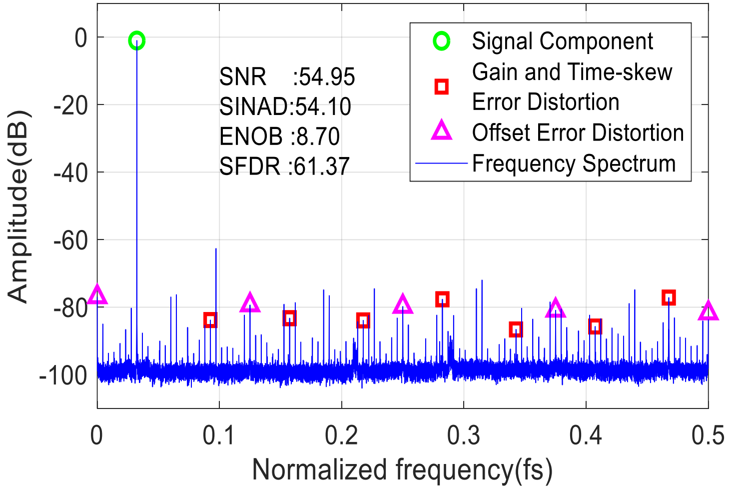
20-Gsps 12-bit TIADC verification system



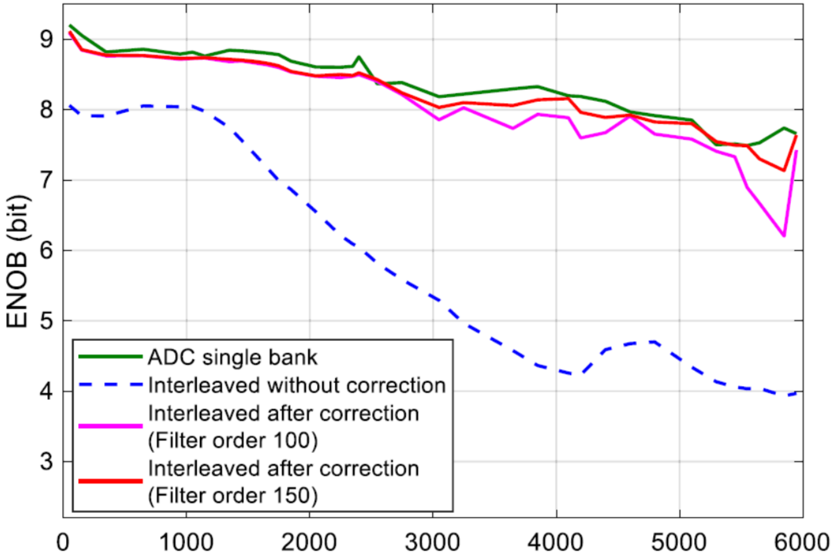




647 MHz before correction



647 MHz after correction



The mismatch errors have been effectively eliminated within a wide bandwidth range.

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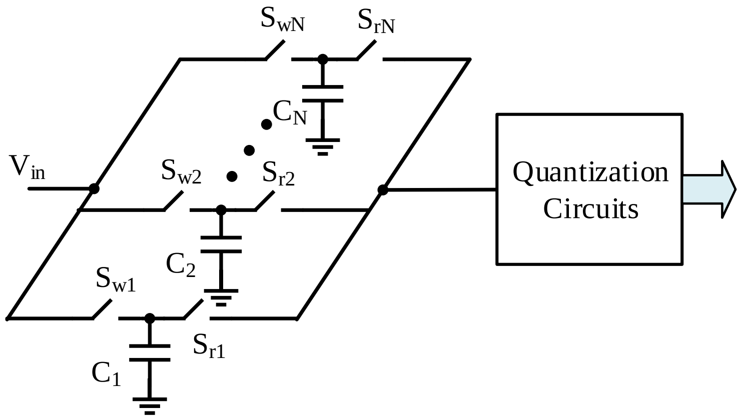
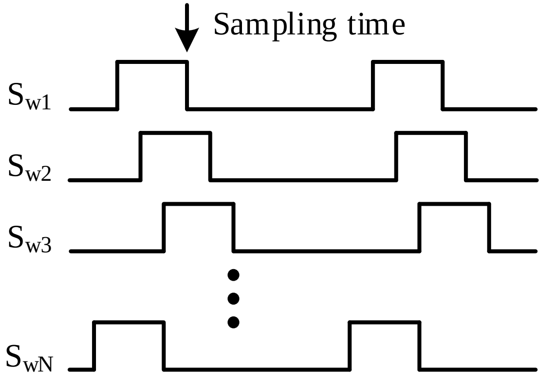
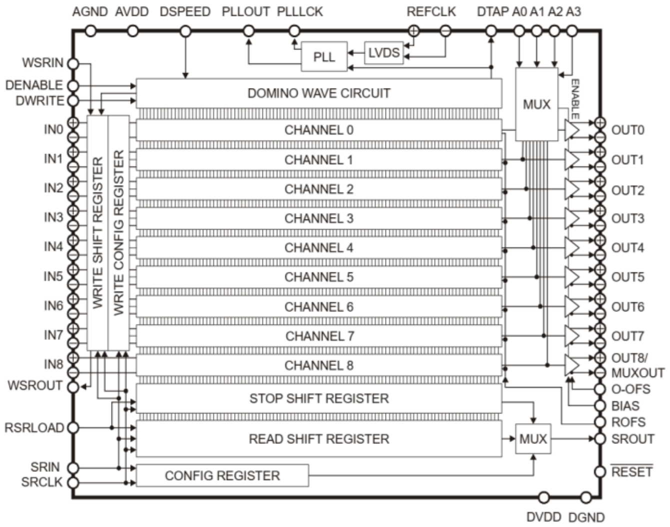
Switched Capacitor Array

- SCA Operating Principle





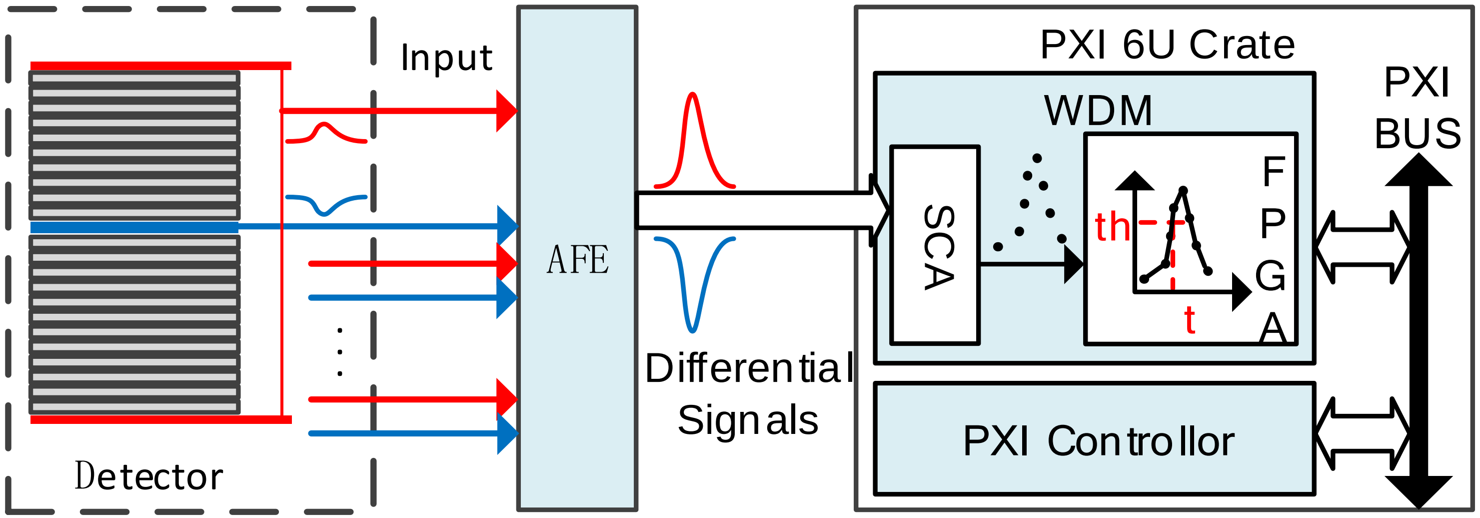
- DRS4 ASIC



Parameters	Value
Sampling rate	0.7 ~ 6 Gsps
Number of channel	8+1
Sampling Depth	1024
Input Range	1 V
Voltage Noise	0.35 mV RMS
Analog BW	950 MHz

DRS4 based Waveform Digitization Electronics

◆ Electronics structure

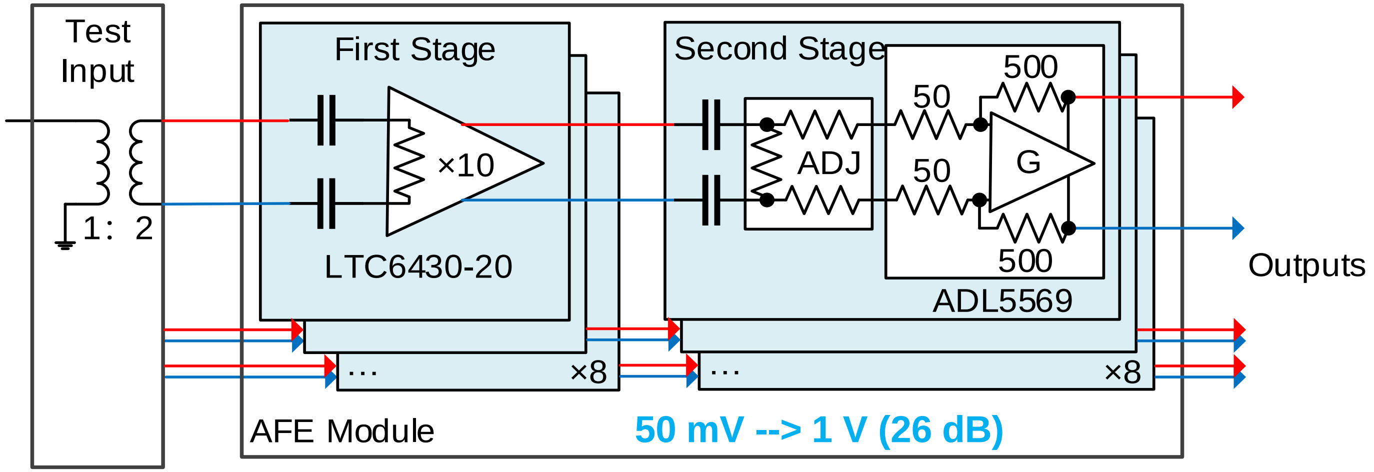


- Analog Front-end Electronics (AFE)
  - Low noise, high bandwidth preamp
  - Placed close to detectors

- Waveform Digitization Module (WDM)
  - DRS4 ASICs
  - ADCs
  - FPGA

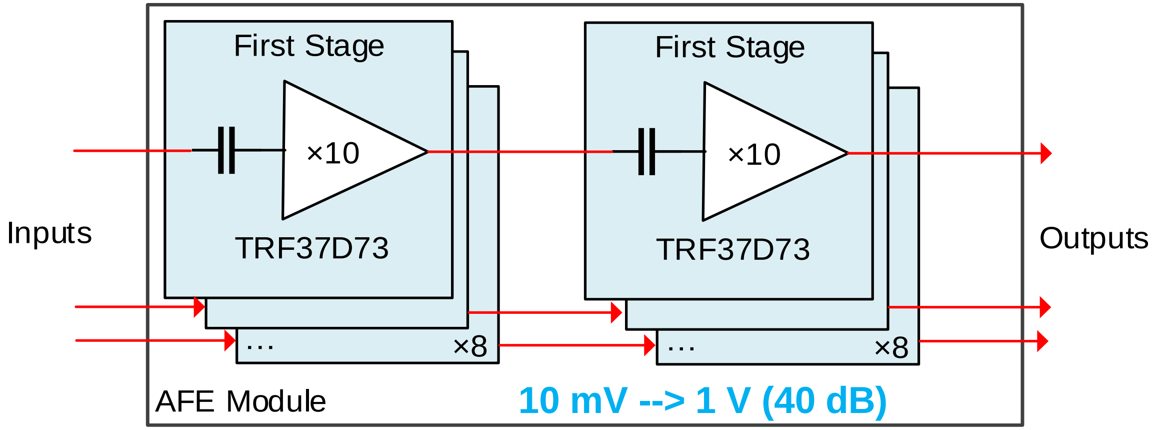
Analog Front End

- AFE for MRPC
  - Full differential
  - First Stage
    - ✓ RF amplifier, 20 dB gain
    - ✓ Ultralow noise, high bandwidth
  - Second Stage
    - ✓ OPA, adjustable gain



AFE for MRPC Detector

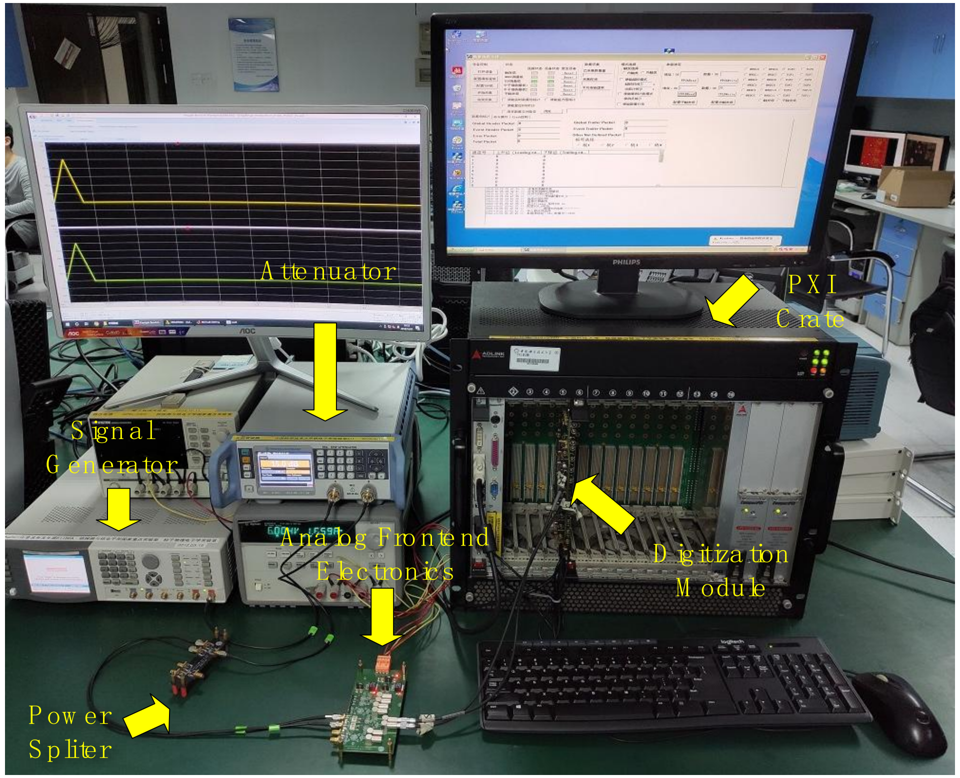
- AFE for PICOSEC-Micromegas
  - Single-end
    - ✓ RF amplifier, Fixed gain
    - ✓ Ultralow noise, high bandwidth



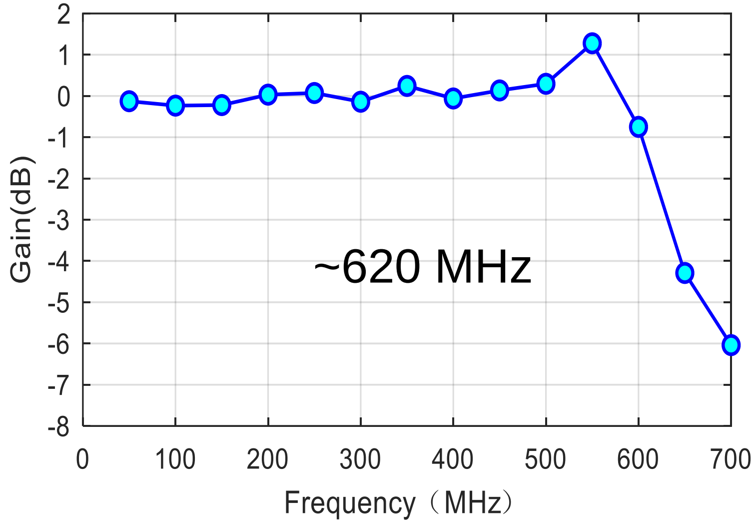
AFE for PICOSEC-Micromegas Detector

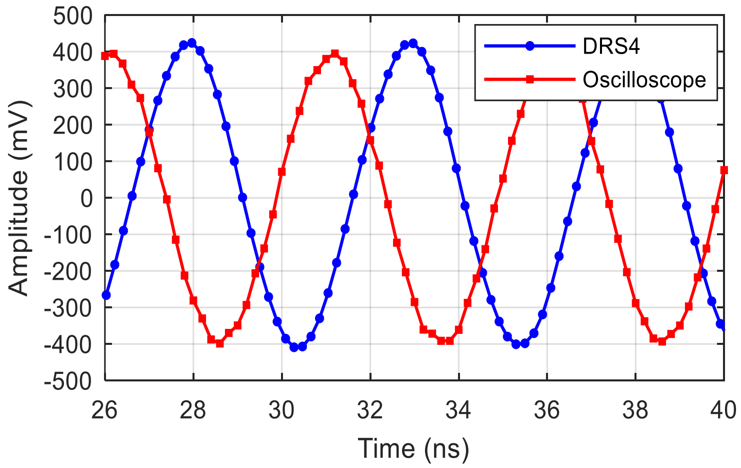
Test Results

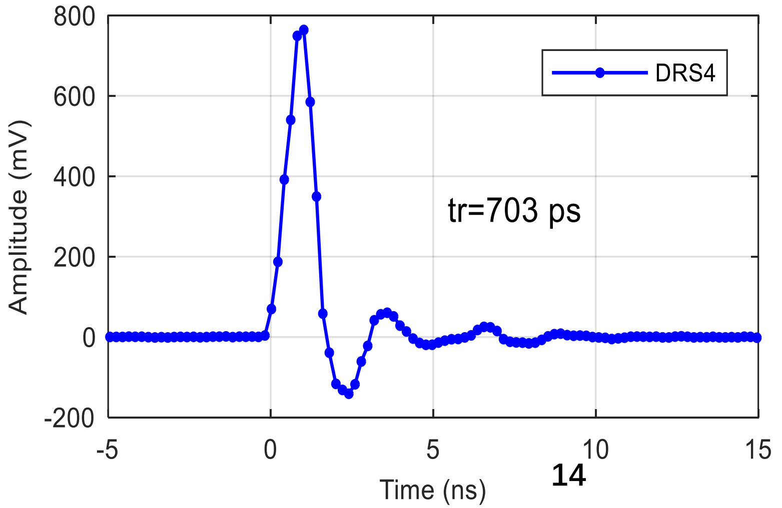
- Waveform capture



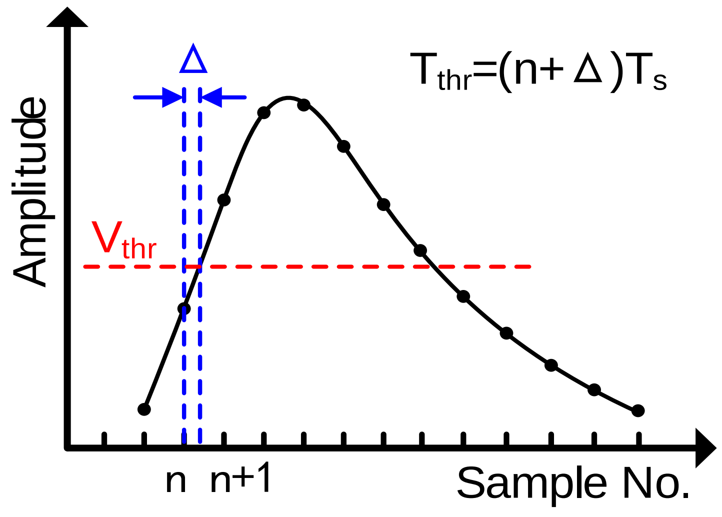
Oscilloscope: Lecroy 760 Zi-A
- 6 GHz ABW
- 5 Gsps (40 Gsps)



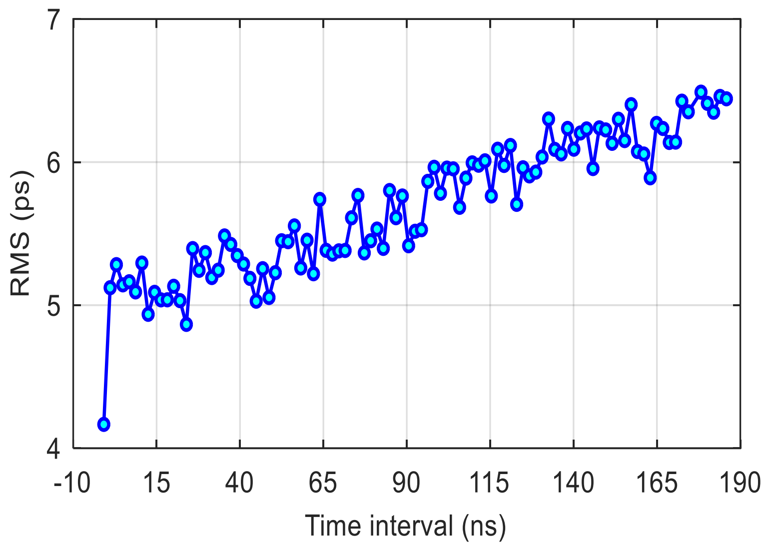




Test Results

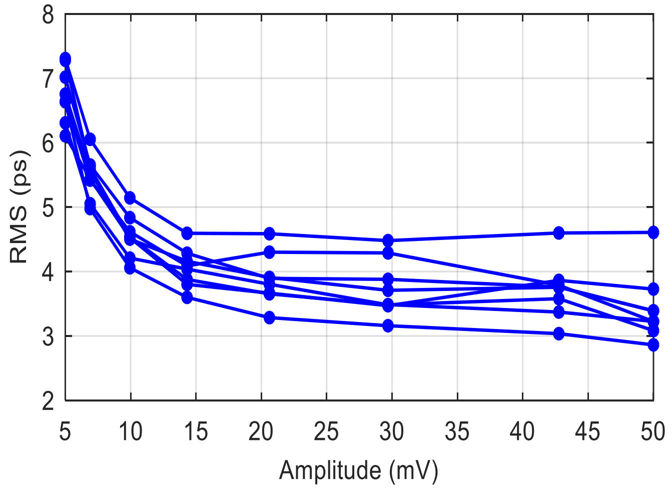


- Time resolution of Digitization Module

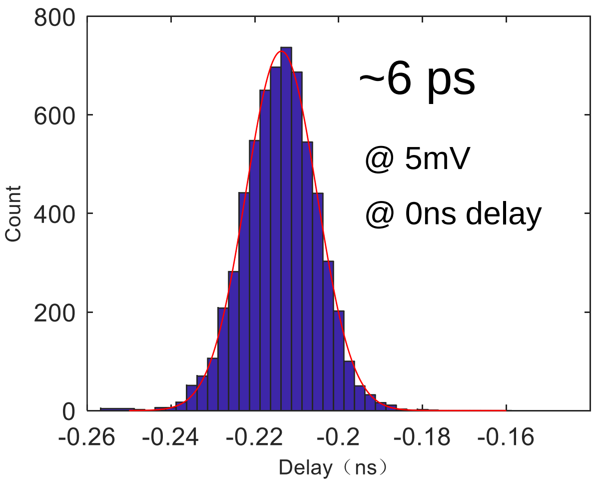


- Time resolution of readout electronics (AFE + WDM)

For MRPC

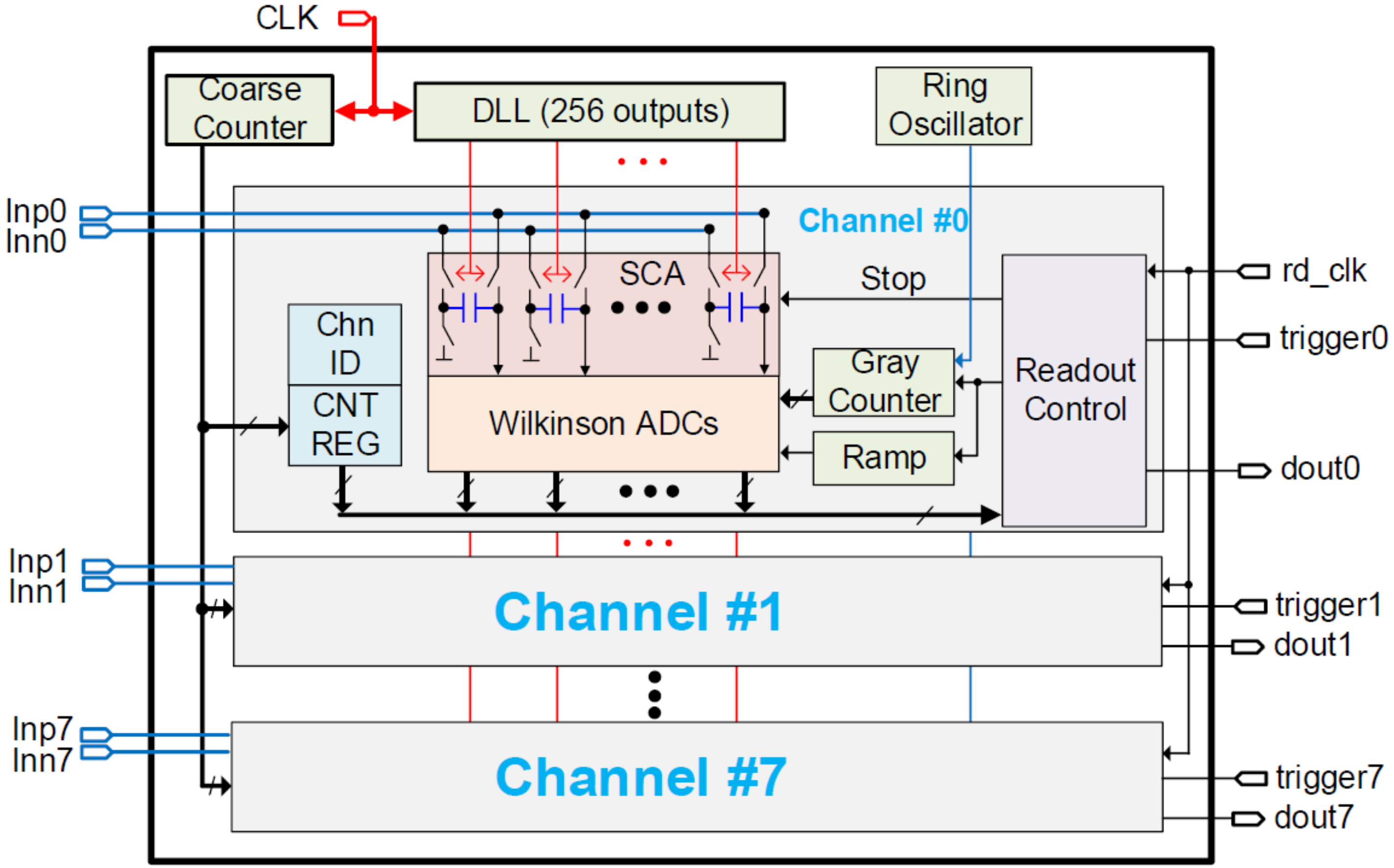


For Micromegas



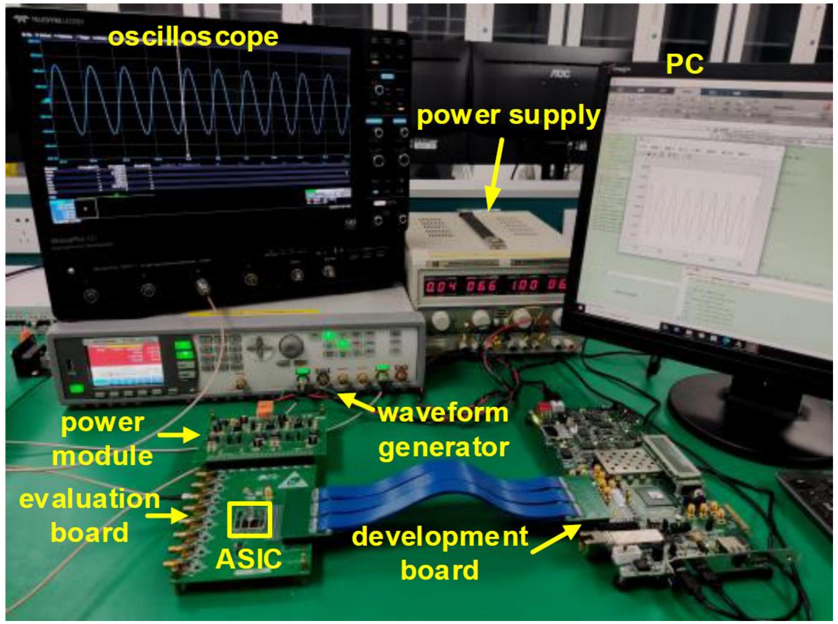
Self-developed SCA ASIC

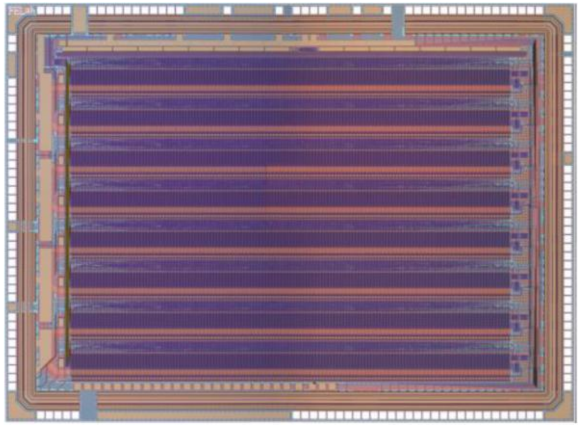
- To integrate the A/D converter into the ASIC
- To implement the independent trigger for each channel

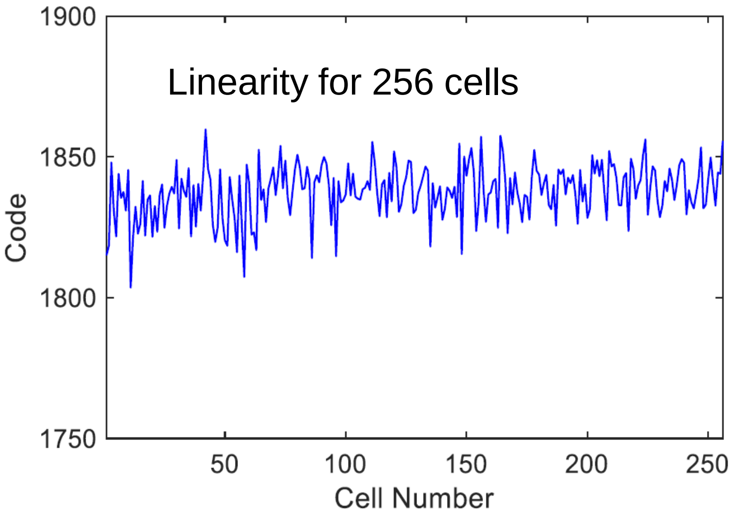


Parameters	Value
Sampling rate	1~5 Gsps
Number of channel	8
Sampling Depth	256
Input Range	1 V
Voltage Noise	< 1 mV RMS
ADC resolution	12 bits @ 1 GHz
Conversion time	4 μs
Trigger	External

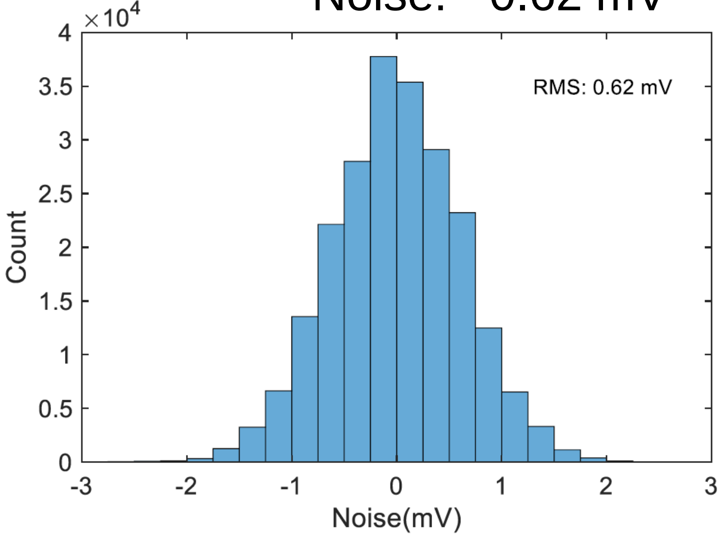
Test Results – DC performance

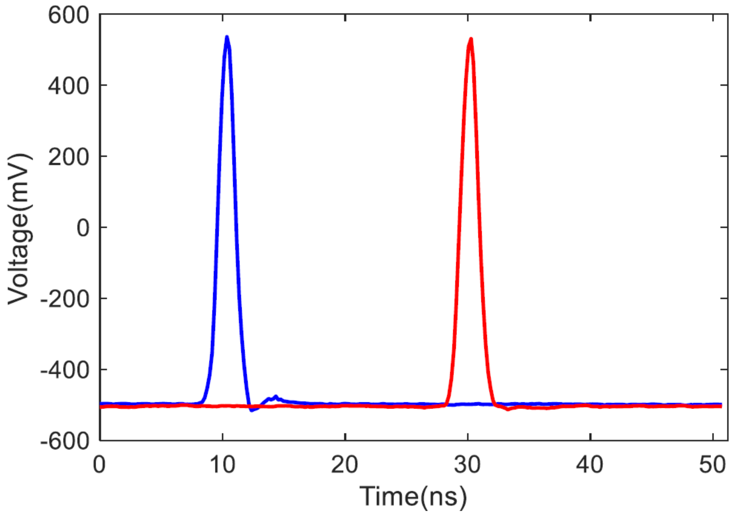


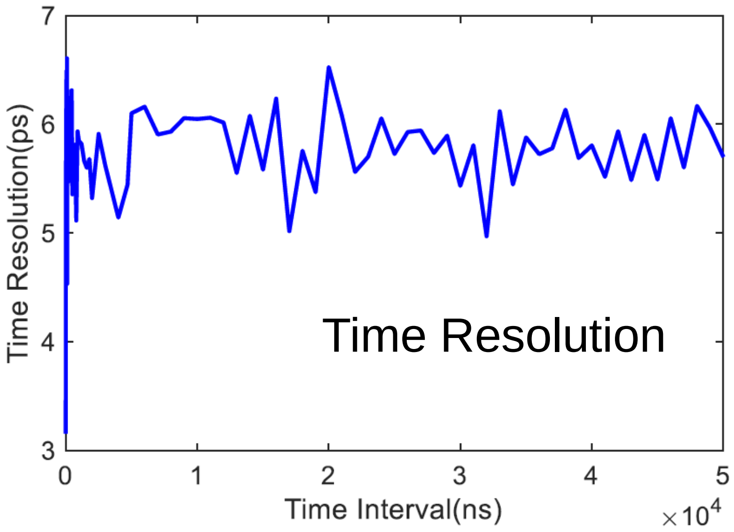




Noise: ~0.62 mV







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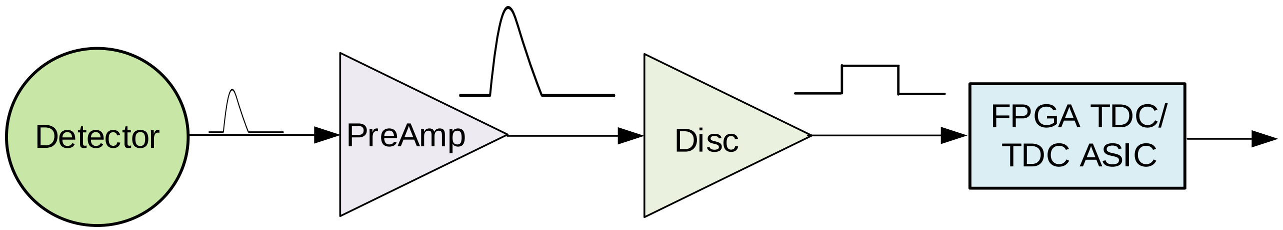
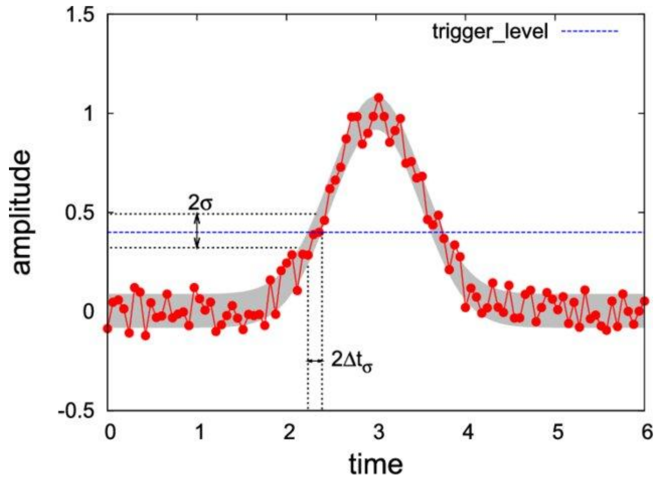
Jitter Contribution



$$jitter_{electronics} = \sqrt{jitter_{a\,\&\,d}^2 + jitter_{TDC}^2}$$

Amp & Disc jitter



$$jitter_{a\&d} = \frac{V_{noise}}{V_{sig}} \times t_r$$

- Low noise (improve SNR)
- High slew rate

TDC jitter

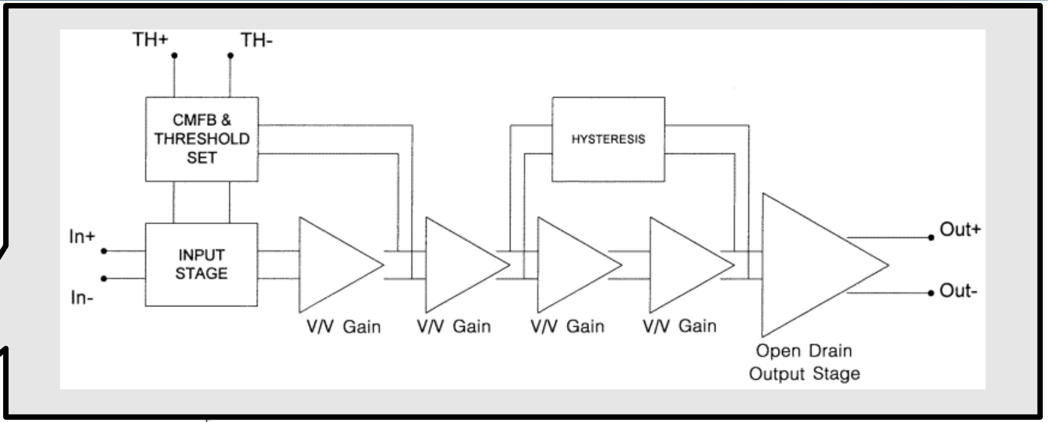
$$jitter_{TDC} = \sqrt{jitter_q^2 + jitter_{noise}^2 + jitter_{clock}^2}$$

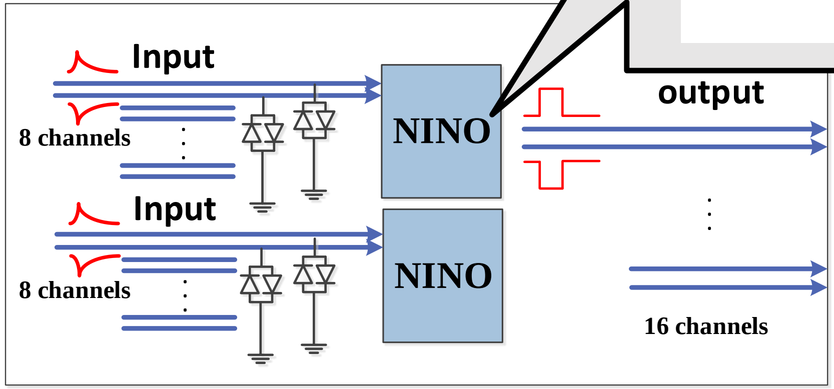
$$jitter_q = 0.5 \times \frac{T_{LSB}}{\sqrt{2}} \approx 0.35T_{LSB}$$

- Small TDC bin size
- Low clock jitter

Amplification and Discrimination

NINO ASIC





parameters	performance
Signal Range	100fC-2pC
Noise	< 5000 e- rms
Power	< 30 mW/ch
Output interface	LVDS

- Input impedance matching
- Saturation amplification with 4-stage amplifiers
- Adjustable threshold voltage
- Low noise, low power consumption
- Pulse stretcher (pulse with > 10 ns)

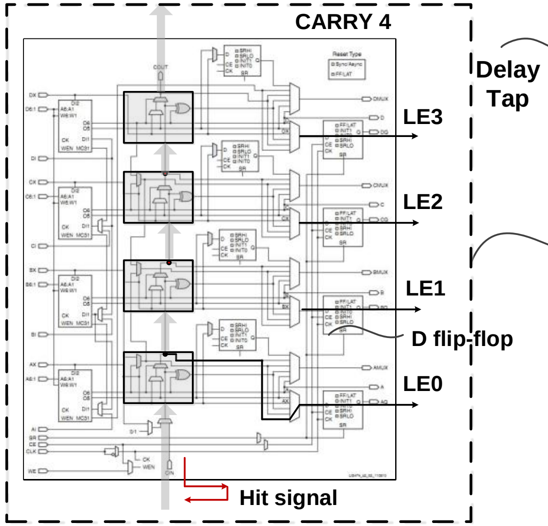
FPGA TDL TDC

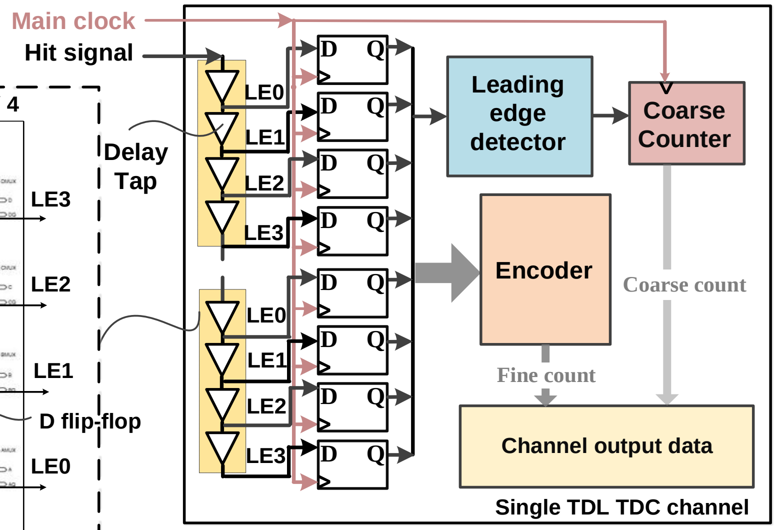
TDL(Tapped delay line) TDC

- Dedicated fast carry chain
- DFFs sample the state of the chain
- Encoding and readout

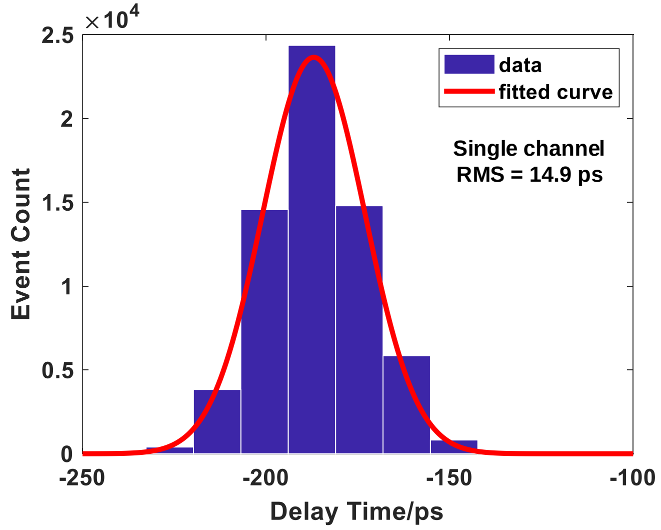
XC7A200T FPGA

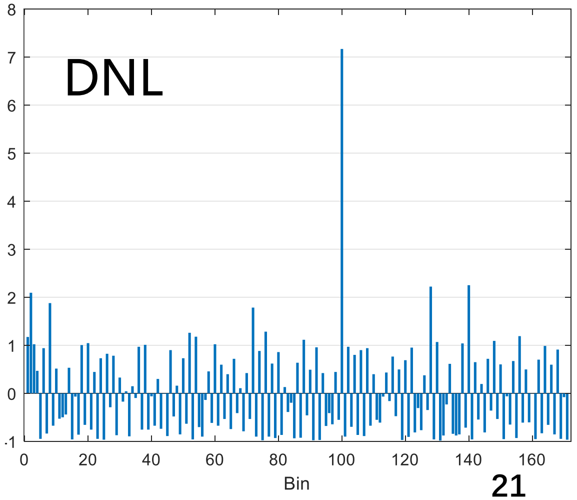
- CARRY4, four taps
- Average bin size is ~18 ps
- Initial precision: ~15 ps





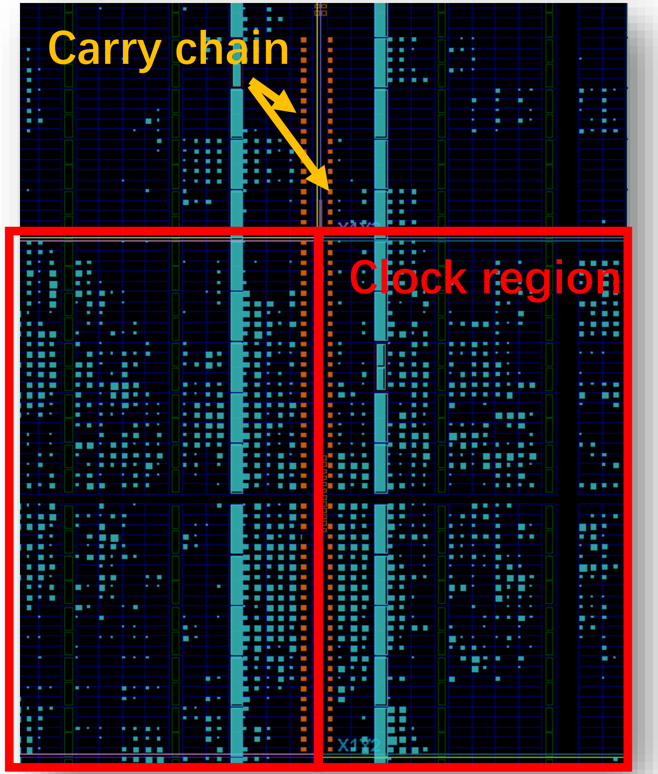
$$T_{arrival} = T_{coarse} - n \times LSB$$

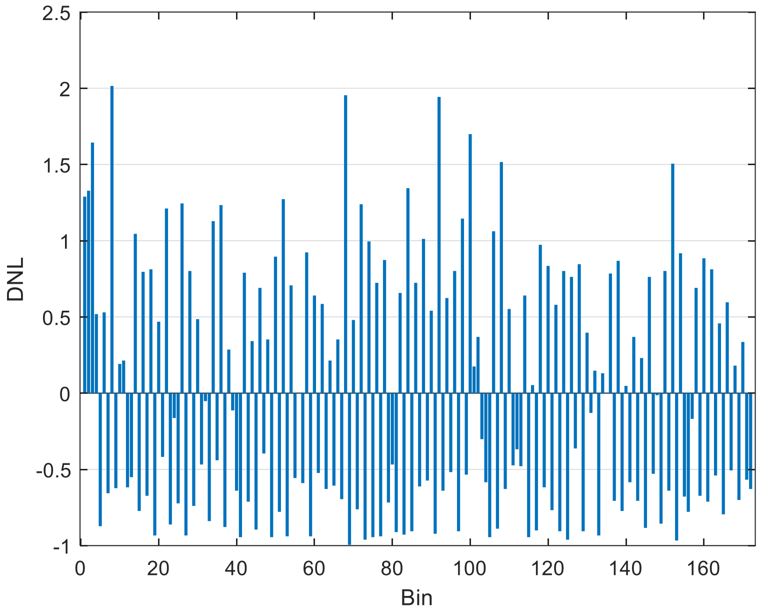


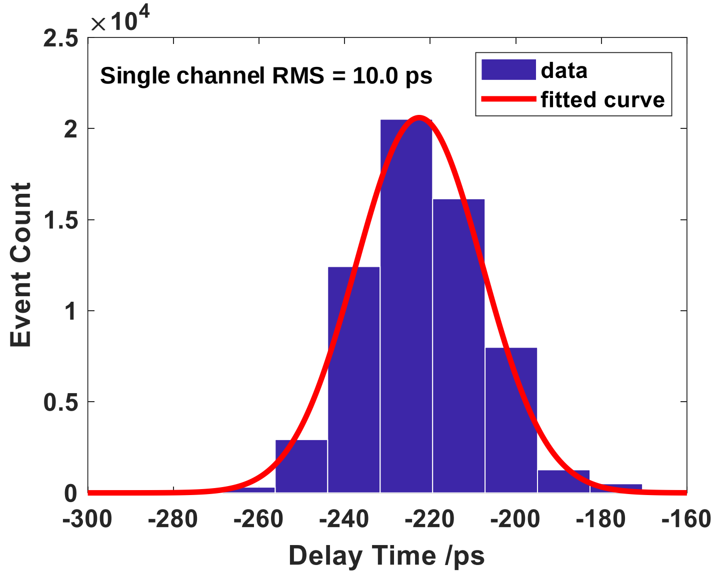


Precision Improvement (1)

Ultra-wide bin elimination







- Constrain the TDL within a clock region
  - Start from the bottom of a clock region
  - Choose a proper clock frequency (>300 MHz for Artix-7 FPGA)

~10 ps precision is achieved

Precision Improvement (2)

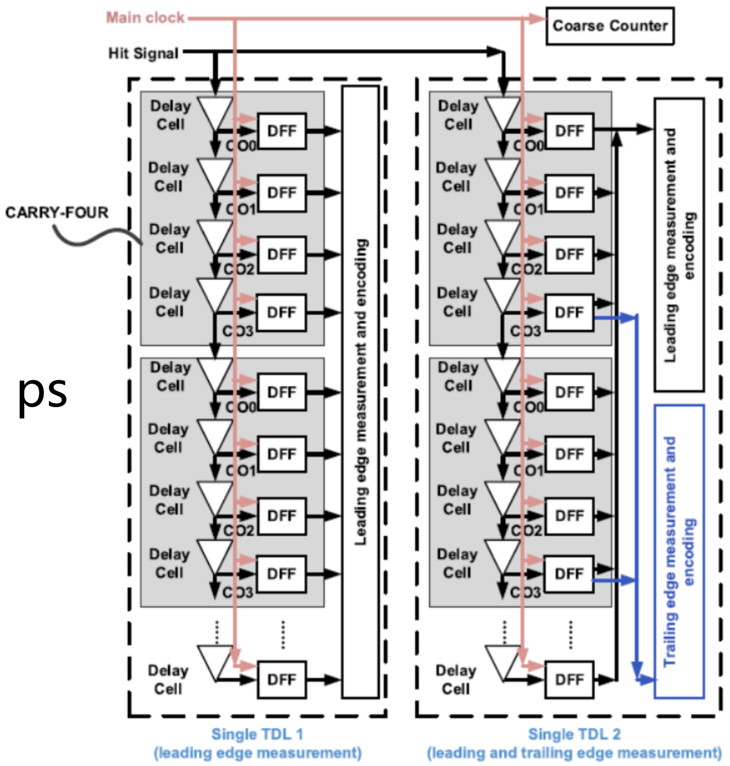
Further improve the precision

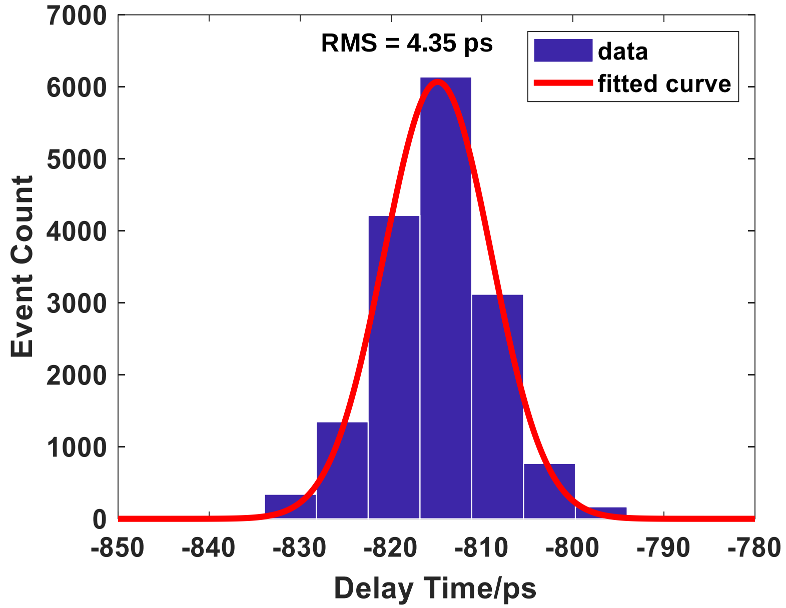
Reduce the bin size

- Upgrade the FPGA
  - Artix-7 -> Kintex-7
  - Averaged bin size: 18 ps -> 12 ps

Multi-measurement

- Multiple parallel TDC
- Double-chain

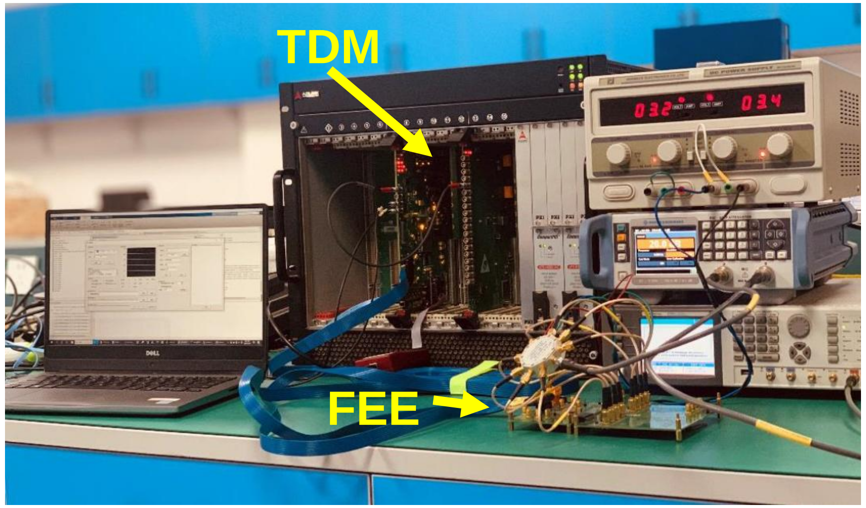


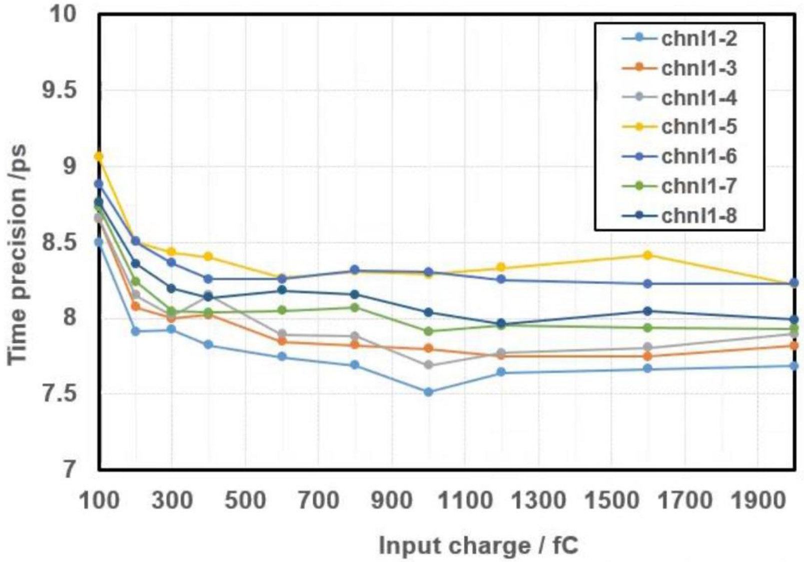


XC7K325T
Clock frequency: 480 MHz

~4 ps precision is achieved

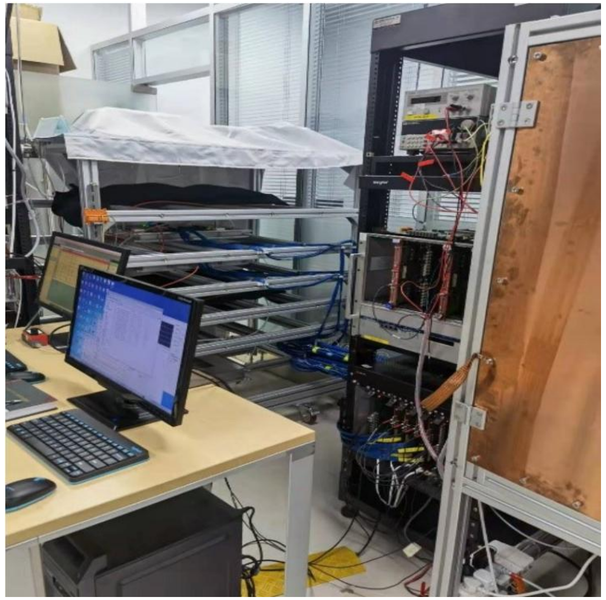
Test Results

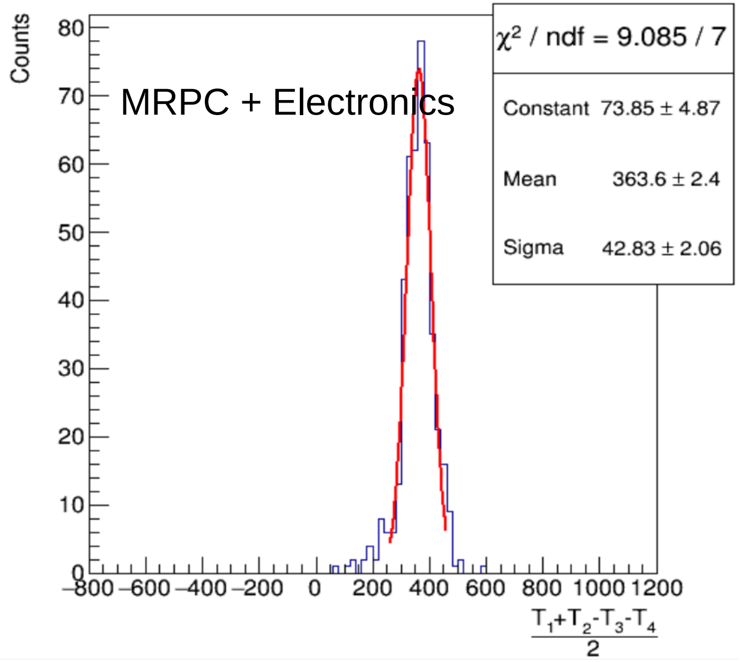




Electronics precision: < 10 ps

- 100 fC-2 pC





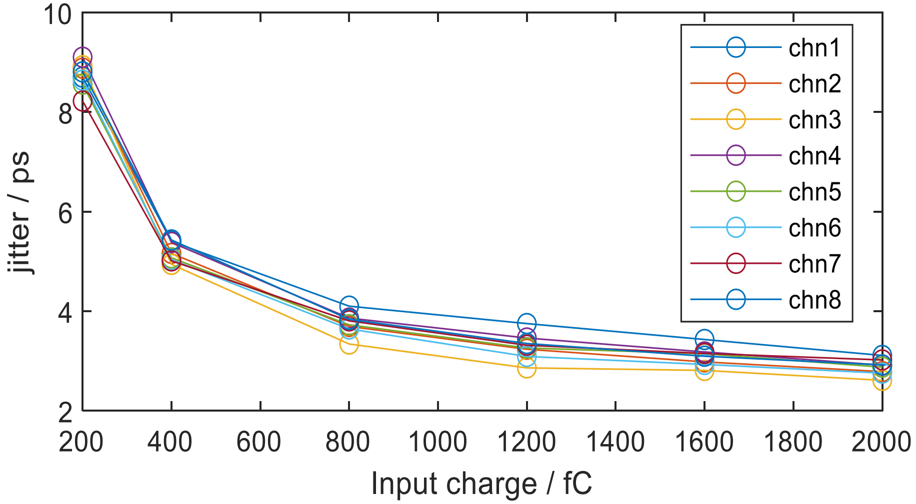
Time precision: ~ 30 ps

- Cosmic test
- ToF between two layers
- with time walk correction

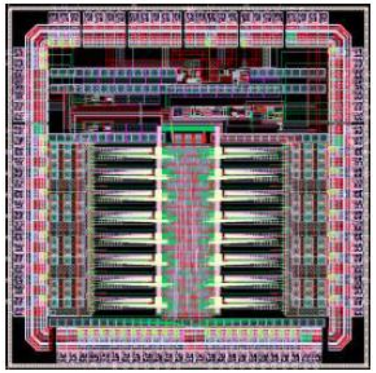
Self-developed ASICs

Amplification and Discrimination ASIC

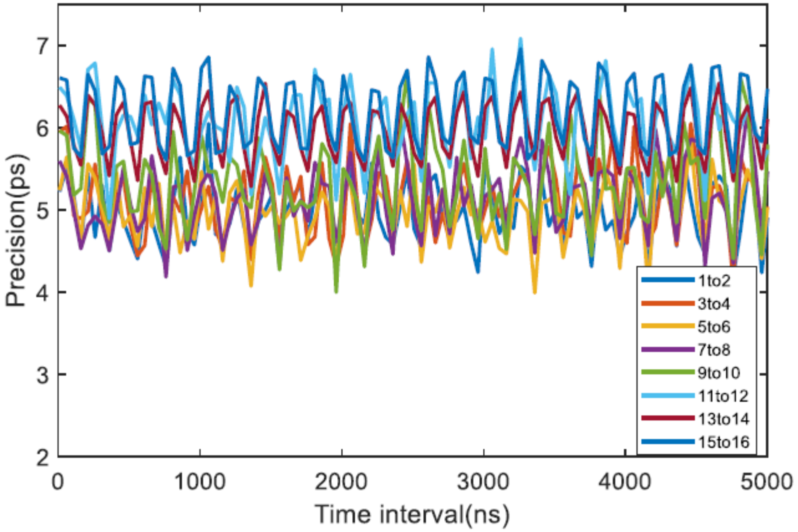
	Performance
CMOS process	180nm
Number of channels	8
Input impedance (Ω)	40~200
Jitter (ps, RMS)	<10
Power consumption (mW / chn)	<25



TDC ASIC



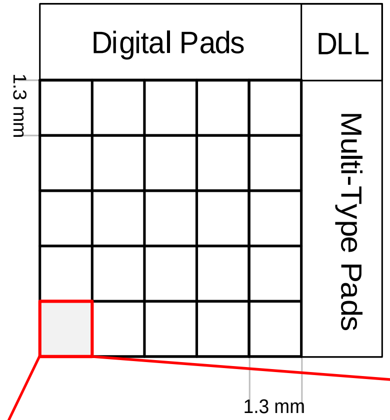
	Performance
CMOS process	180nm
Number of channels	16
Dynamic range	5.12 µs
precision	< 7.5 ps

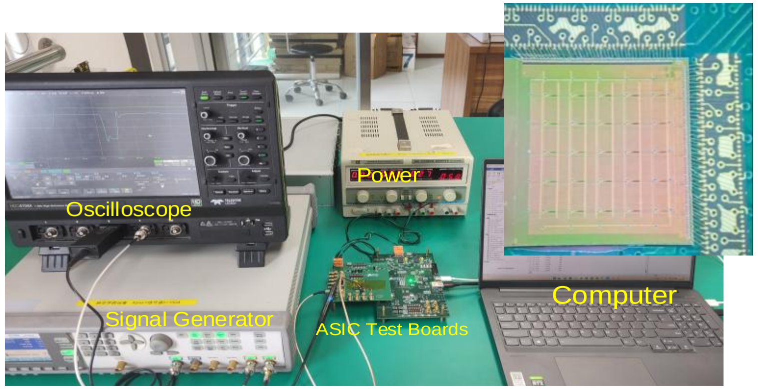


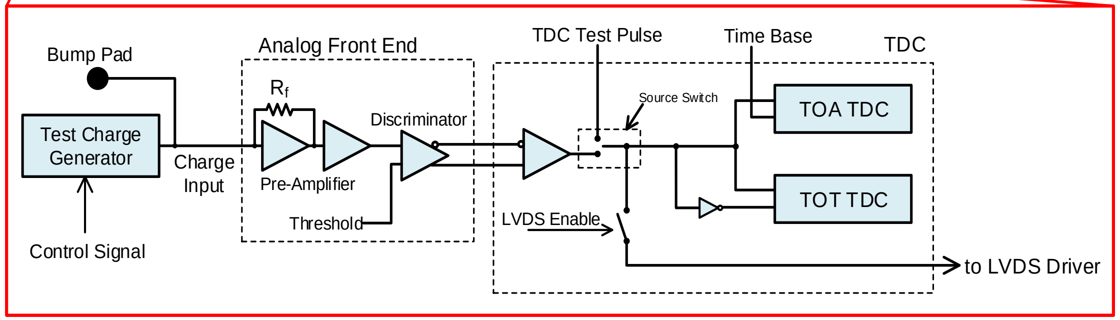
Self-developed ASICs

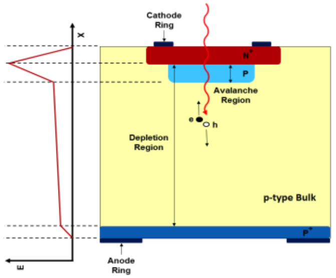
LATIC: LGAD Amplification and Timing IC(A readout ASIC for LGAD sensor)

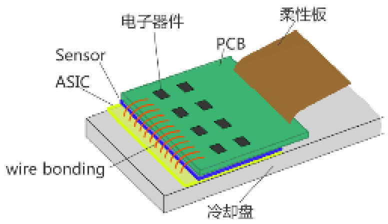
- 5×5 prototype
- TDC： jitter < 10ps
- Analog + TDC： jitter < 20ps @10fC 4pF

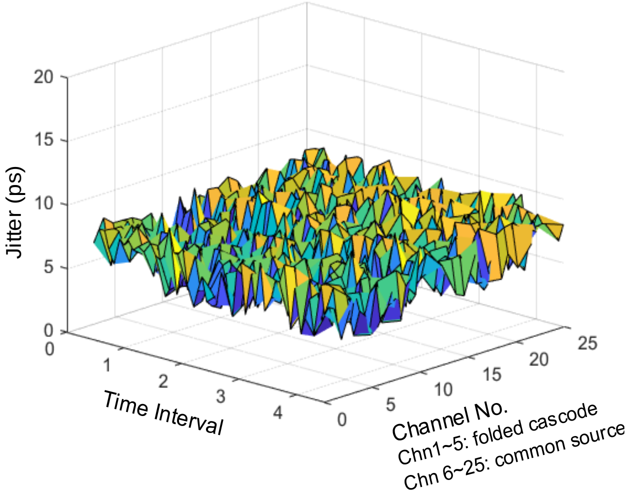


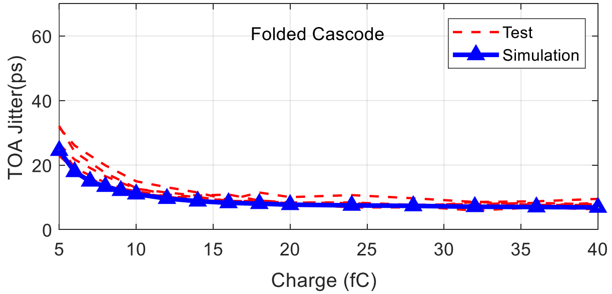












Summary

- TIADC based waveform digitization
  - Proposed a broadband mismatch error correction method
  - A 20-Gsps 12-bit TIADC system is designed and evaluated
- DRS4 based waveform digitization electronics
  - Better than 10 ps RMS timing resolution is achieved for MRPC and PICOSEC-Micromegas signals
- FPGA-TDC based high precision time measurement electronics
  - Double-chain FPGA TDC with Kintex-7 : ~ 4ps RMS
  - NINO + FPGA-TDC: < 10 ps @ 200 fC~2 pC
- Self-developed ASIC
  - SCA ASIC: 5 Gsps sampling rate, < 7 ps RMS
  - Amplification and Discrimination ASIC： < 10 ps RMS, @200 fC-2 pC
  - TDC ASIC: < 7.5 ps RMS

Thank you for your attention !