Contribution ID: **502** Type: **Poster**

High Speed 5GSps Pulse Shape Digitization Prototype Based on RFSoC

Wednesday 27 August 2025 18:00 (2 hours)

High-speed and high-precision pulse waveform digitization has extremely high application value in many fields such as nuclear physics experiments and medical imaging. The requirement for capturing picosecond-level pulses in the China Jinping Neutrino Experiment also poses extremely high demands on the pulse sampling rate. However, traditional solutions are mostly based on board-level circuits, adopting an architecture of analog pre-conditioning + high-speed ADC + FPGA (DSP) processor, which leads to high system complexity, low integration, high power consumption, and high design difficulty, and performs poorly in terms of system noise and high-speed transmission. To address these issues, this paper developed a high-speed pulse waveform digitization prototype based on RFSoC, achieving 5 GSps (Giga Sample per second) high-speed pulse waveform digitization. RFSoC integrates field programmable logic controller (PL), multi-core processor subsystem (PS), and eight-channel 5GSps/14-Bit analog-to-digital and 9.85GSps/14-Bit digital-to-analog converters (RFDC) in a single chip. Experimental results show that the high-speed pulse waveform digitization prototype based on RFSoC fully retains the pulse time-domain characteristics and can meet the strict requirements of dynamic range and time accuracy with 9.10-Bit ENOB at 347MHz input, 9.14-Bit at 10MHz input and 4GSps (compare to 8.56-Bit ENOB at 347MHz with ADC12DJ5200RF from TI). Compared with discrete solutions (4-Chip of ADC12DJ5200RF for 8-Channel 5GSps/12-Bit ADC with XCVU3P FPGA), this prototype reduces power density by 40%, reduces occupied area by 60%, and achieves sub-picosecond-level multi-channel synchronization accuracy, demonstrating extremely high application value in the field of high-speed pulse waveform digitization.

Collaboration you are representing

Authors: BIAN, Zhenxue; Mr XUE, Tao; Mr YANG, Haoyan; LIANG, Bo; WEI, Liangjun; LIU, Yinong; LI, Jianmin

Presenter: BIAN, Zhenxue

Session Classification: Poster session

Track Classification: Underground Laboratories – Technology