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Design of RFSoC Based Hardware Module for Electronics System of Frontier Physics Experiments.

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The high-speed integrated data converters and digital data processing capability in RFSoC empower direct RF sampling without analog mixer up and down conversion for RF frequencies up to 5 GHz with more compact footprint and lower total power consumption and cost. This work reports the hardware design methodology of RFSoC, the power sub-system which include 80-A 0.85V core supply with dual phase DC-DC in used and 72-Bit DDR4 SDRAM is implemented for PS sub-system. At the same time, dual 16-Bit DDR4 SDRAM is designed for PL sub-system. For the footprint optimization, dual side mounted (Top and Bottom) DDR4 chips topology is used and capacitive-compensation signal integrated method is used. 8-Channel 5 GSps/14-Bit ADC and 8-Channel 9.85 GSps/14-Bit DAC high-speed analog differential signals are fan-out with Samtec ADM/ADF high-speed and high-density connectors. While the 8-Channel 25 G-bit GTY transceivers are all fan-out with the same connectors. The compact size of this module is 70mm plus 96mm and which is suitable for readout and control system with state-of-the-art microwave SQUID multiplexers, and also capable for the digitalization of MCP PMT with 200-ps rising time.

Collaboration you are representing

Authors: Mr WEI, Liangjun (Tsinghua University); Prof. XUE, Tao (Tsinghua University); Mr YANG, Haoyan (Tsinghua University); Mr LIANG, Bo (Tsinghua University); Ms CUI, Na (Tsinghua University); Mr CHEN, Xiantao (Tsinghua University); Prof. LI, Jianmin (Tsinghua University); Prof. LIU, Yinong (Tsinghua University)

Presenter: Mr WEI, Liangjun (Tsinghua University)

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