

Fast front-end readout design for NICA-MPD shashlik electromagnetic calorimeter

摘要

硅光电倍增器 (SiPMs) 因其出色的光响应和高增益特性而备受青睐, 但其在快速定时应用中的使用常受到其高端接电容 (通常超过 300 pF) 的限制。在电磁量热器中, 亚纳秒级的时间测量使这些探测器能够作为辅助的飞行时间设备使用, 特别是在 NICA-MPD 实验中, 目标时间分辨率为 150 皮秒。

为应对这些挑战, 本研究提出了一种新颖的前端读出电子学设计, 采用两级共基极跨阻前置放大器和一个 12 位、200 MS/s 的流水线逐次逼近寄存器 (SAR) 模数转换器 (ADC)。利用 Hamamatsu S13360-6025 作为输入源进行的大量 SPICE 仿真显示, 该前置放大器具有快速的上升时间和良好的线性度。激光测试的实验结果证实, 该快速前置放大器设计实现了优于 20 皮秒的卓越时间分辨率。

ADC 电路采用 TSMC 65nm 低功耗工艺设计, 采用两级流水线 SAR 结构, 并引入了两步转换技术 (6 位 +7 位), 在第二步中包含冗余设计。在 160 MHz 采样率和 80 MHz 输入条件下进行的测试显示, 在 $V_{pk} = -1\text{dBFS}$ 时, ADC 的 FFT 频谱分析得到了 9.34 的有效位数 (ENOB) 和 73.8 dBc 的无杂散动态范围 (SFDR)。

在 200 MHz 采样率下进行的初步系统级时间评估表明, 对于上升时间为 15 至 20 纳秒的波形, 在上升沿具有 3 至 4 个采样点的情况下, 时间分辨率约为 20 皮秒。

关键词

快速前置放大器, 前端读出电子学, 时间分辨率

Abstract

Silicon photomultipliers (SiPMs) are highly valued for their excellent light response and high gain characteristics, yet their application in fast timing scenarios is often limited by their high terminal capacitance, typically over 300 pF. In electromagnetic calorimeters, sub-nanosecond time measurements allow these detectors to function as supplementary time-of-flight devices, specifically aiming for a time resolution of 150 ps in the NICA-MPD. To address these challenges, this study proposes a novel front-end readout electronics design featuring a two-stage common-base transimpedance preamplifier and a 12-bit 200 MS/s pipelined successive-approximation-register (SAR) analog-to-digital converter (ADC). Extensive SPICE simulations, using the Hamamatsu S13360-6025 as the input source, demonstrate the preamplifier's rapid rise time and good linearity. Experimental results from laser testing confirm that this fast preamplifier design achieves a remarkable time resolution of better than 20 ps. The ADC circuit, designed using the TSMC65nmLP process, employs a two-stage pipelined SAR structure with a two-step conversion technique (6-bit + 7-bit), incorporating redundancy in the second step. Testing at a 160MHz sampling rate with an 80MHz input condition showed that, at $V_{pk} = -1\text{dBFS}$, the ADC's FFT spectrum analysis yielded an effective number of bits (ENOB) of 9.34 and a spurious-free dynamic range (SFDR) of 73.8 dBc. Preliminary System-level timing assessments under a 200 MHz sampling rate revealed that waveforms with 3 to 4 sampling points on the rising edge, with a rise time of 15 to 20 ns, achieved a time resolution of approximately 20 ps.

Keywords

fast pre-amplifier, front-end readout, time resolution

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Session Classification: 海报展示

Track Classification: 02 海报展示: 海报展示