High-speed and high-precision pulse digitization electronics system with high-bandwidth readout for frontier physics experiments

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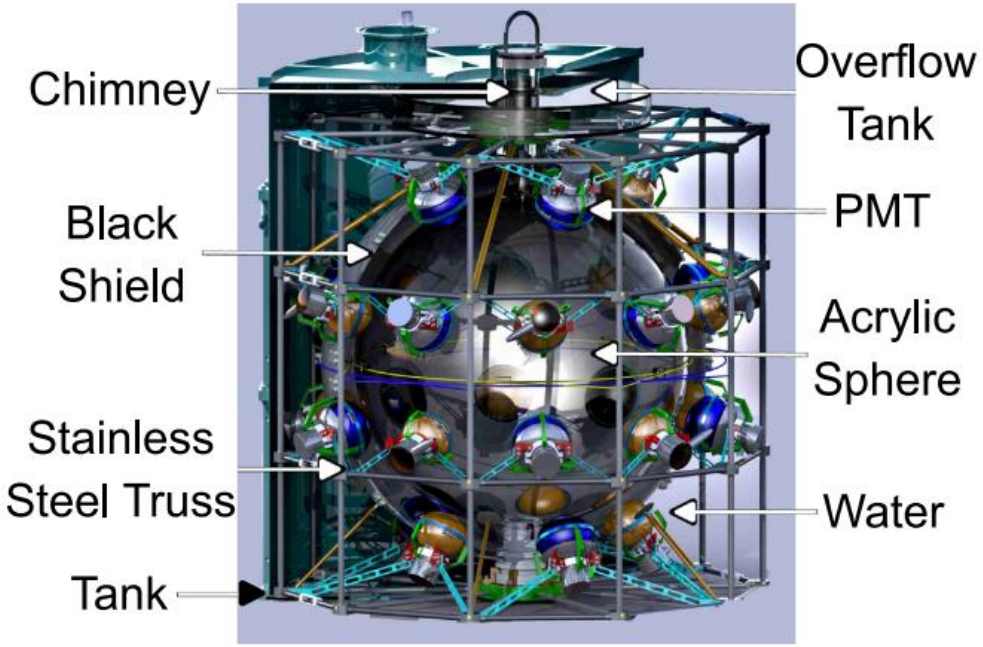
Context

- Introduction
- Hardware Design
- Performance Test
- Conclusion

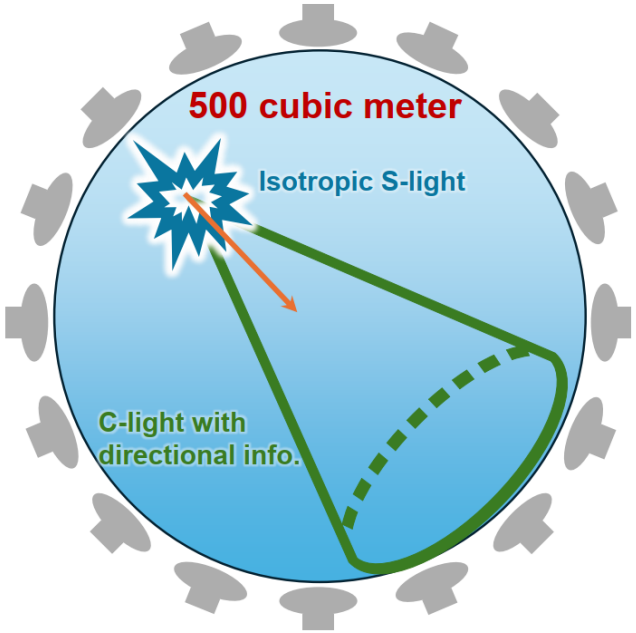
Introduction

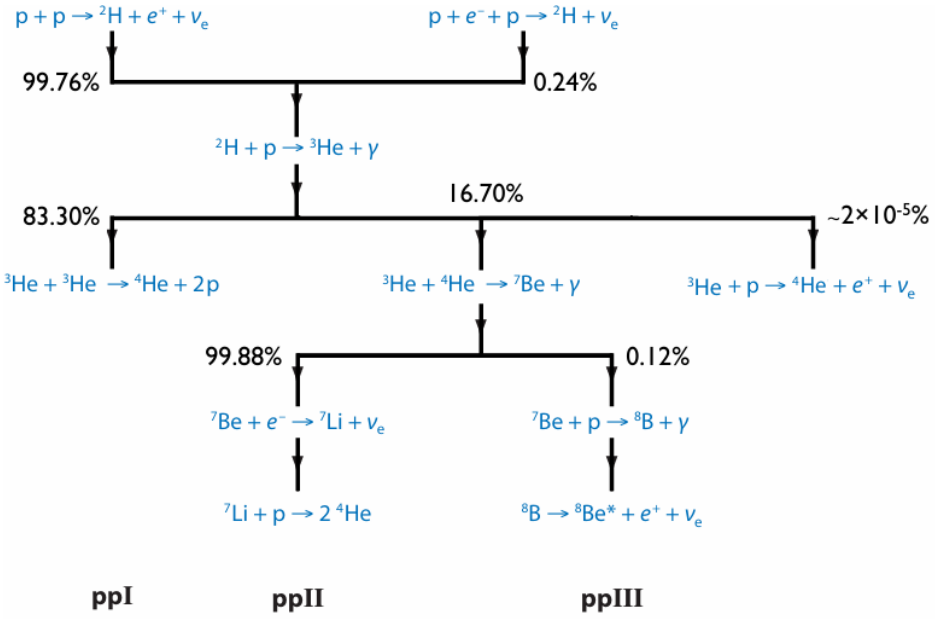
- **Jinping Neutrino Experiment (JNE)**
  - **Conducted within the China Jinping Underground Laboratory**
  - **Solar neutrino, geo-neutrino and supernova neutrino**
  - **60 PMTs mounted on the exterior of the spherical detector**
  - **30 channels -> 60 channels -> 4000 channels**

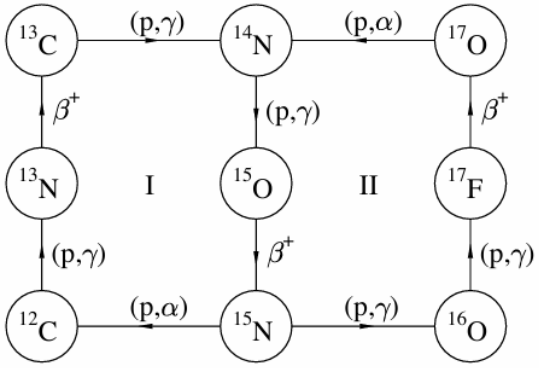


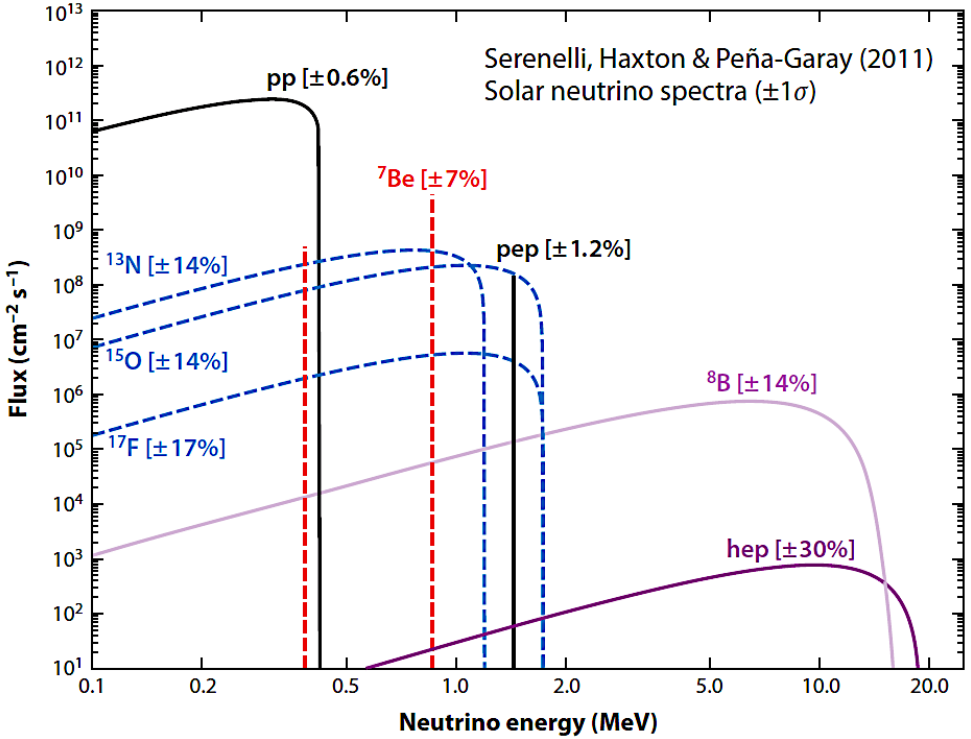
Introduction

- Jinping Neutrino Experiment (JNE)
  - Time resolution
  - Energy resolution
  - Low threshold



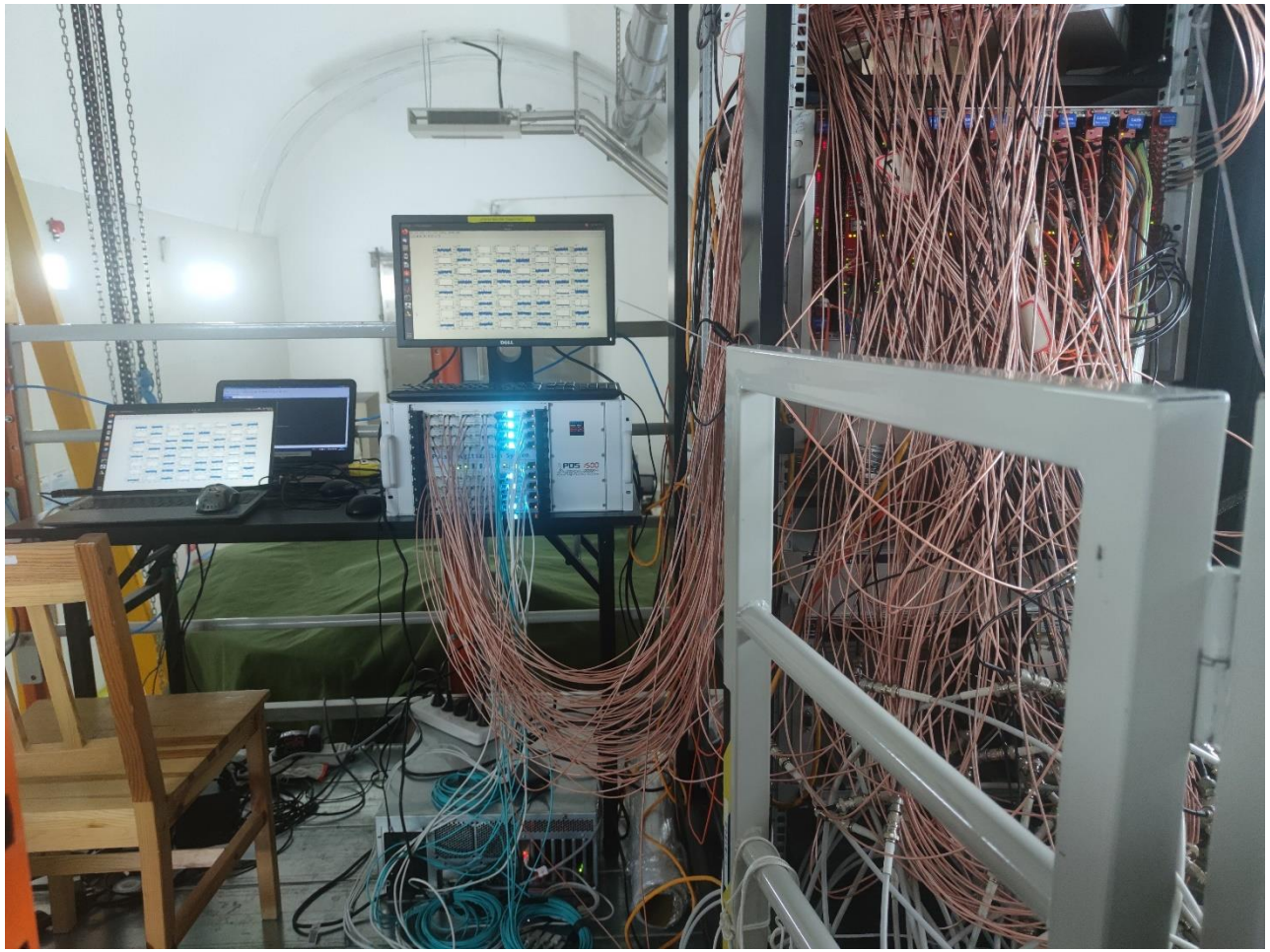






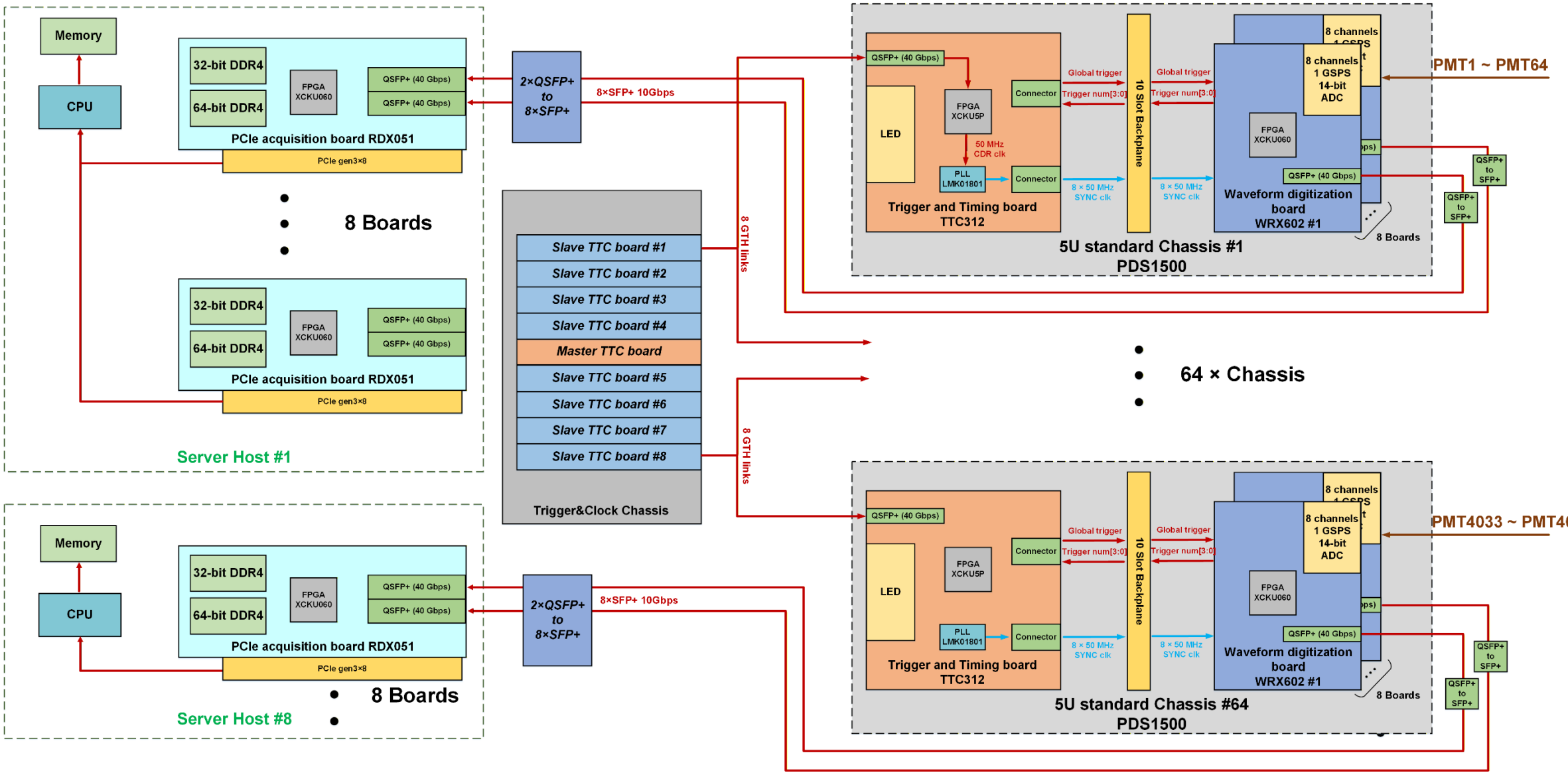
Introduction

- Electronics system
  - Time resolution
    - ADC sampling rate
    - Clock synchronization
  - Energy resolution
    - ADC effective number of bits
  - Low threshold
    - Data transmission bandwidth



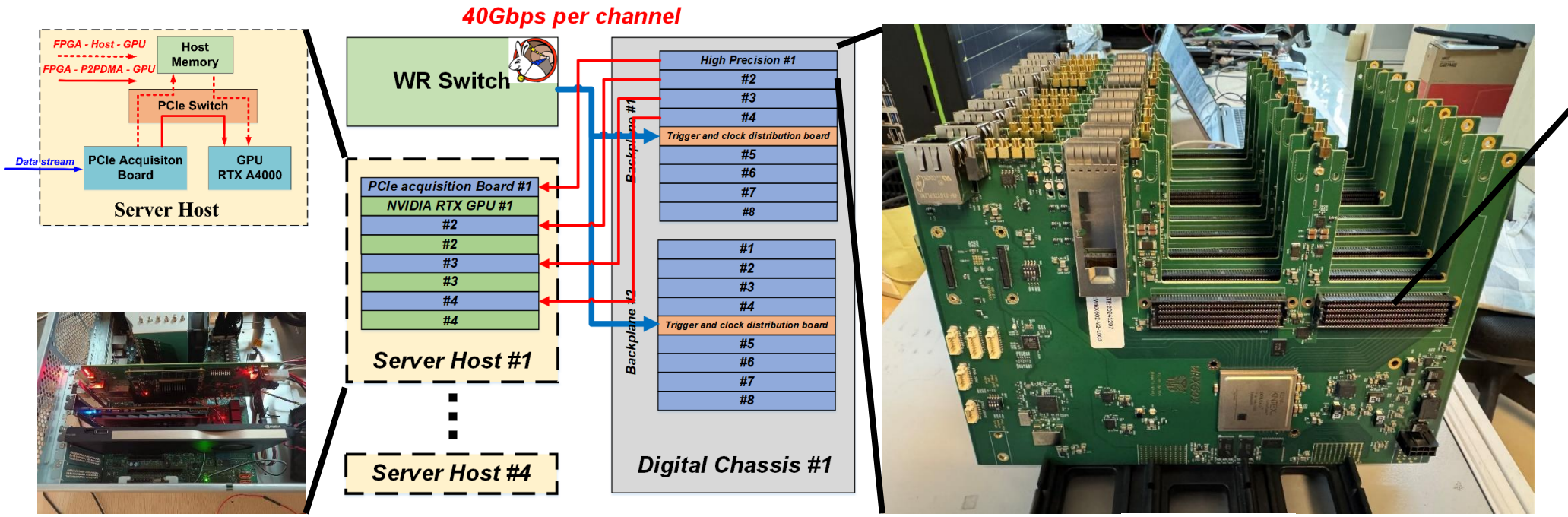
Hardware design

- Tsinghua DAQ system



Hardware design

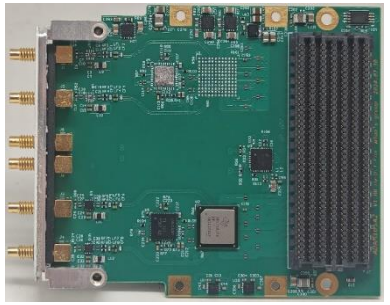
- Tsinghua DAQ system
  - 64 channels 1 GSps/14-bit (Now)、64 channels 5 GSps/12-bit (Future)
  - 64 Gbps QSFP+ per DAQ board (Now)、100 Gbps QSFP28 per DAQ board (Future)



JNE readout system

WRX602

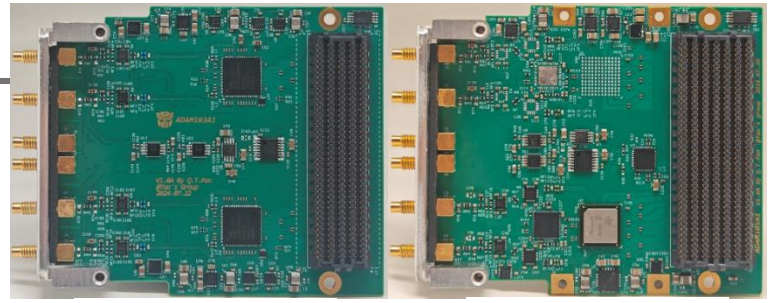
ADAM103A1



ADAM105A2

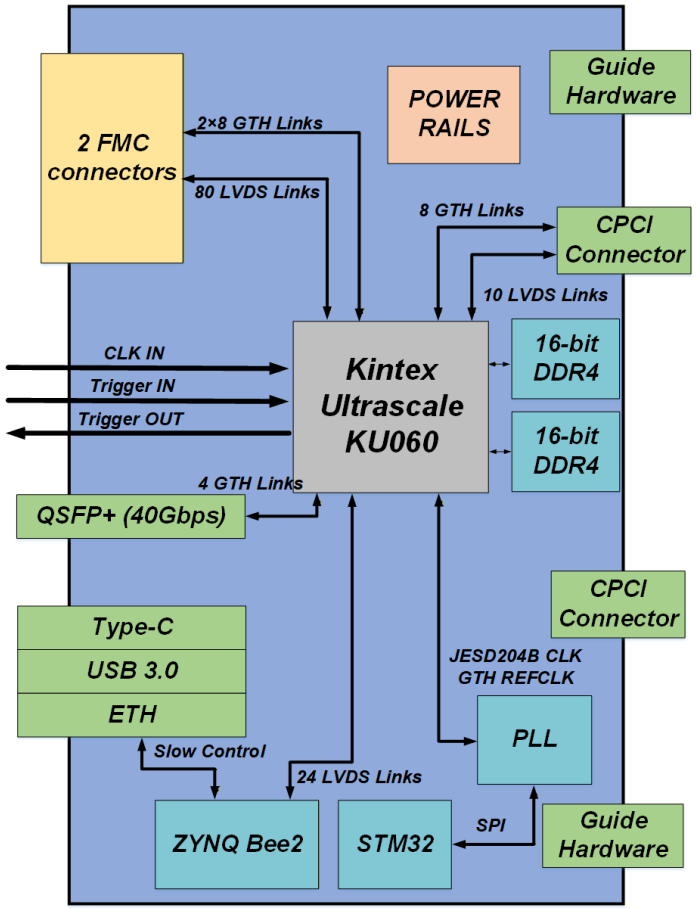
Hardware design

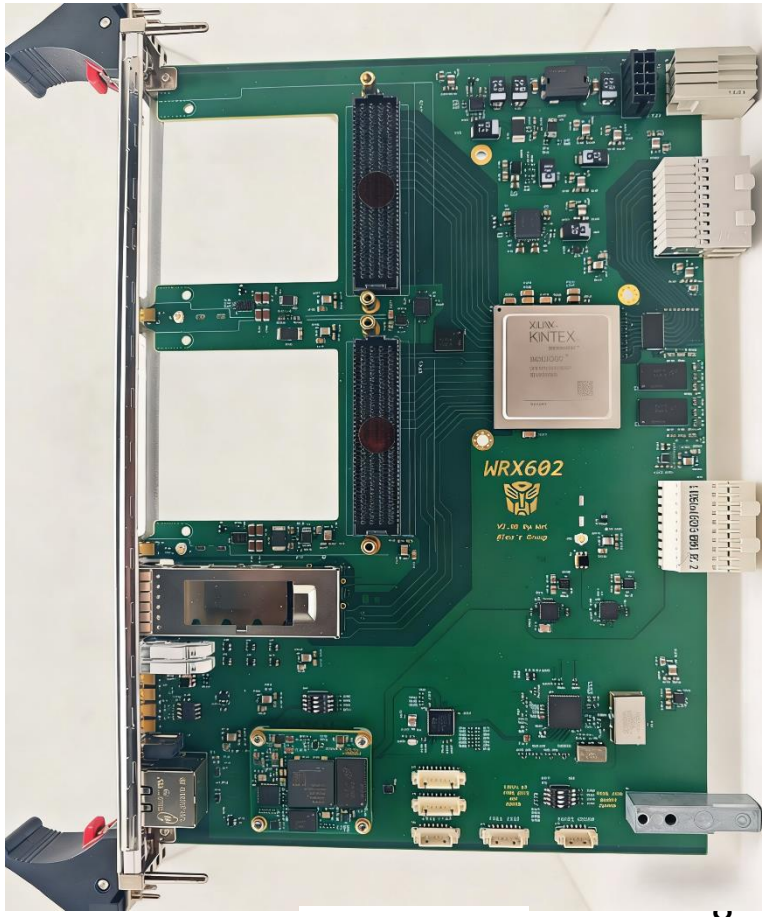
- Tsinghua DAQ system
  - Board of DAQ WRX602
  - Mother board + FMC



ADAM103 ADAM105

	ADAM103 (Main)	ADAM105 (Future)
Channel /Module	4	2/1
ADC	1 GSps 14-Bit	4/8 GSps 12-Bit
Chip	AD9695	ADC12DJ5200RF
Analog Input (Full-Scale)	1.6 Vpp	1.0 Vpp
ADC ENOB（Bit）	~10.6 @ 10 MHz	4 GSps DC：＞8.9 @ 347 MHz
		8 GSps DC：＞8.7 @ 347 MHz

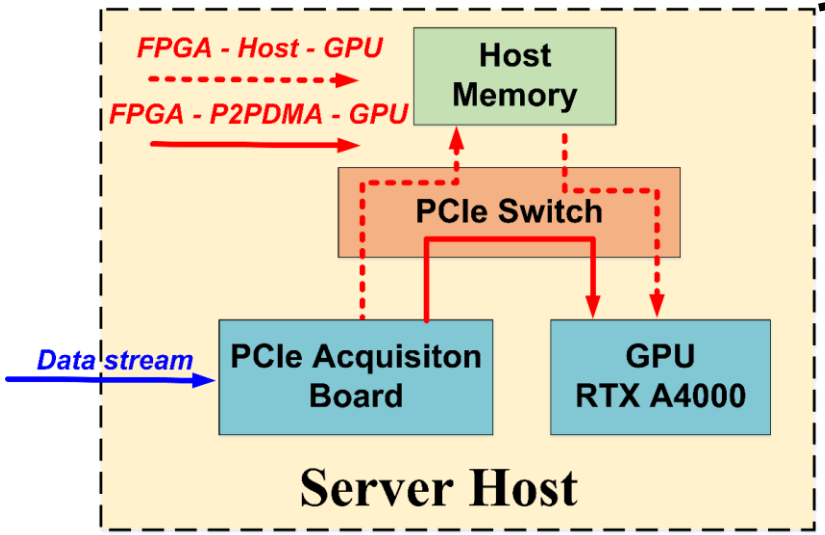


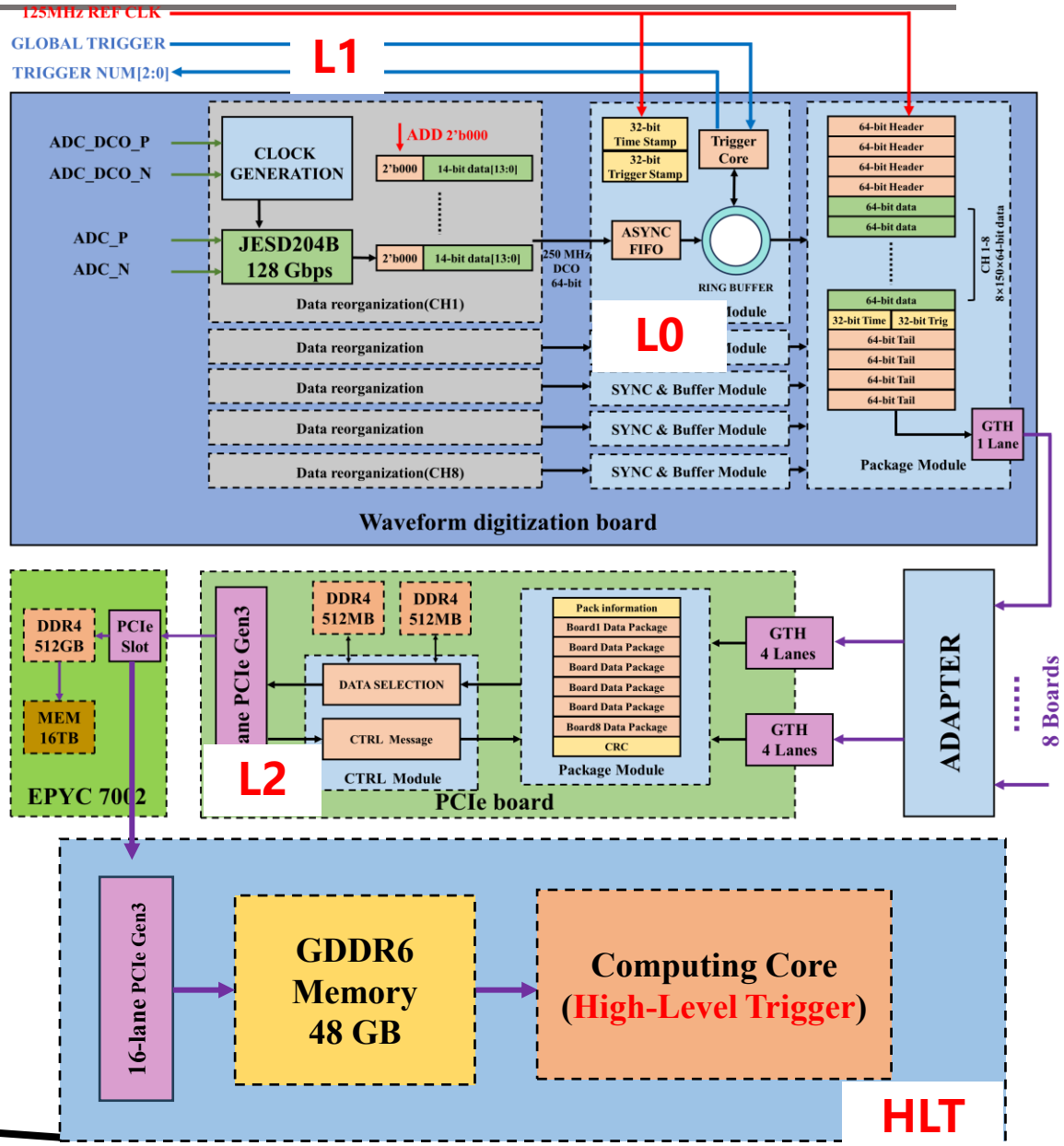


WRX602

Hardware design

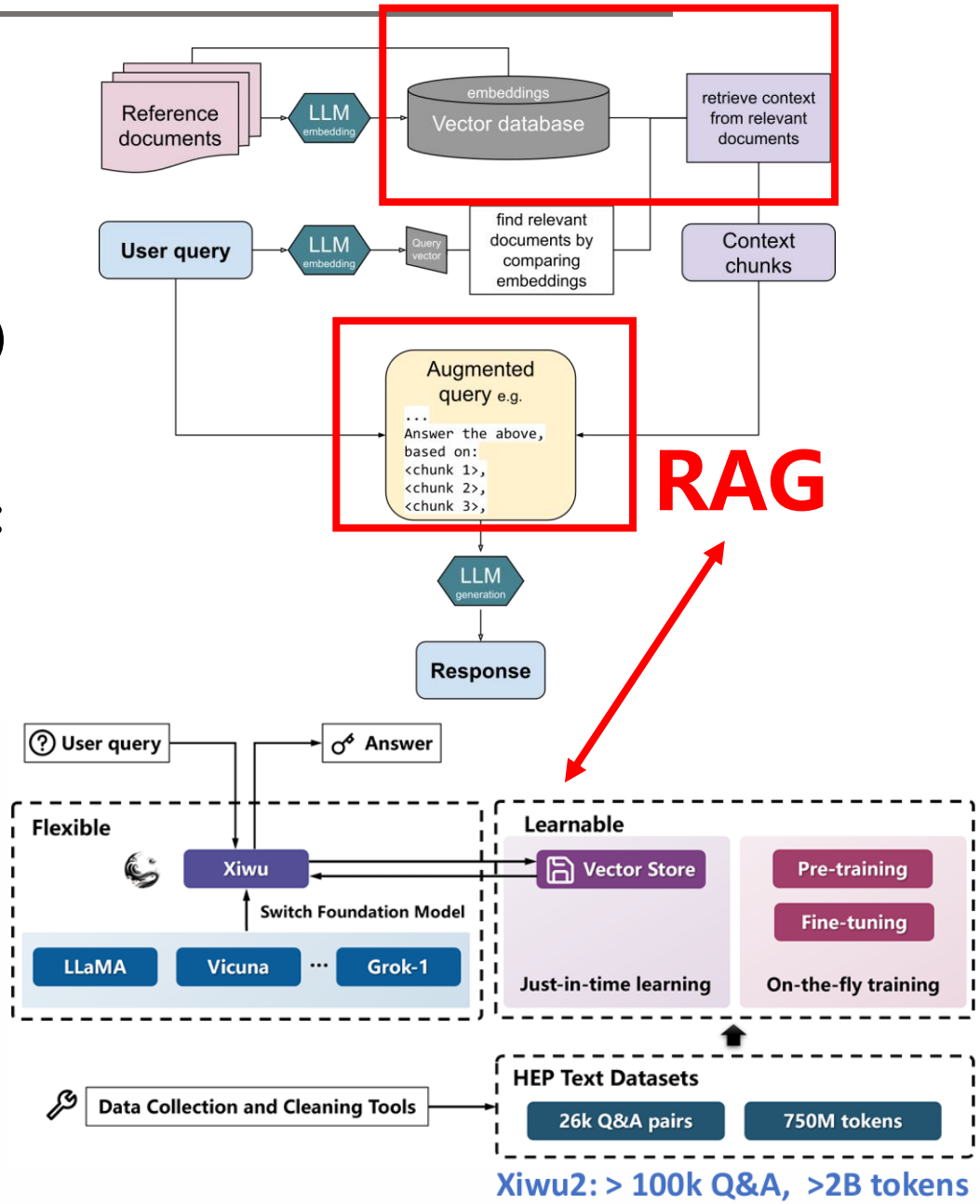
- Tsinghua DAQ system
  - Level 0： Amplitude
  - Level 1： Time
  - Level 2： Energy
  - High-Level





Hardware design

- Tsinghua DAQ system
  - High-Level：综合决策触发-动态
    - Step1：manual control
      - Set parameter→set(ch0,threshold,10)
    - Step2：Requirements Identification
      - Low data bandwidth → "Possibility 1: Threshold set too high; Possibility 2: CHX link failure; Possibility 3…… "
    - Step3：Adaptive exploration
      - Physics research → "Search literature collect data, process results, verify hypotheses, write papers"



Hardware design

- Tsinghua DAQ system
  - High-Level：综合决策触发-动态
    - Step1：manual control
      - Set parameter→set(ch0,threshold

```
[我]（单行指令直接回车，多行列表输入完后请在新行输入 'GO'）:
调整第三块板子的阈值为0x10
[Agent 思考中...]
  --> [触发工具]: semantic_config_daq
      [解析参数]: 板=3, 通道=0, 功能=0x04, 值=0x10
      [硬件抽象层]: 触发规则: 0x04 阈值配置，通道号已被强制修正为 1
  --> [执行结果]:
配置成功！最终拼接的 32-bit 数据为 0x30410010。
底层硬件返回:
device: /dev/xdma0_user, address: 0x10000 (0x10000+0x0), access write.
access width: word (32-bits)
character device /dev/xdma0_user opened.
Memory 0x10000 mapped at address 0x7fb8aa879000.
Write 32-bits value 0x30410010 to 0x10000 (0x0x7fb8aa879000)

[我]（单行指令直接回车，多行列表输入完后请在新行输入 'GO'）:
怎么调节阈值
[Agent 思考中...]
[AI 回复]: 要调节数采系统的阈值，我需要知道以下信息：

1. **板卡号**（0-15）：您要配置哪一块板卡？
2. **通道号**（0-15）：您要配置哪个通道？
3. **阈值配置值**：您希望设置的阈值是多少？（可以是十六进制如 0x1234，或十进制如 4660）

**示例格式**：
- "板卡0，通道1，阈值设置为 0x1000"
- "第3块板卡，第5通道，阈值设为 4096"

请提供这些具体信息，我就能帮您调节阈值。

[我]（单行指令直接回车，多行列表输入完后请在新行输入 'GO'）:
```

```
(agent-env) root@tao:/home/tao/JNE_Agent# python mimo_agent.py
======================================================
  欢迎使用 Tao's Group DAQ AI Agent for JNE（输入 'quit' 退出）
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======================================================

[我]（单行指令直接回车，多行列表输入完后请在新行输入 'GO'）:
调整第三块板子的阈值为0x10
[Agent 思考中...]
  --> [执行结果]:
配置成功！最终拼接的 32-bit 数据为 0x30410010。
```
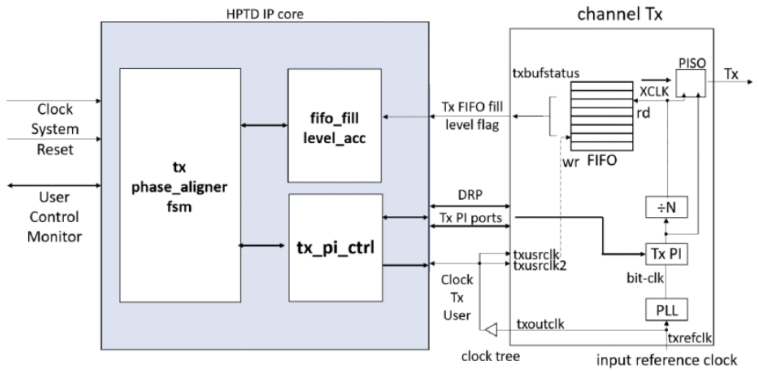
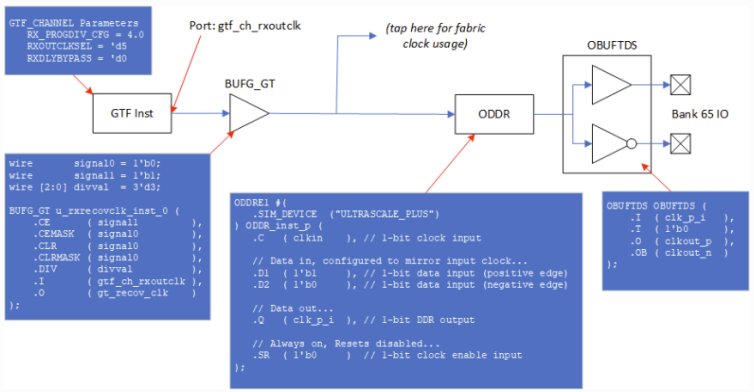
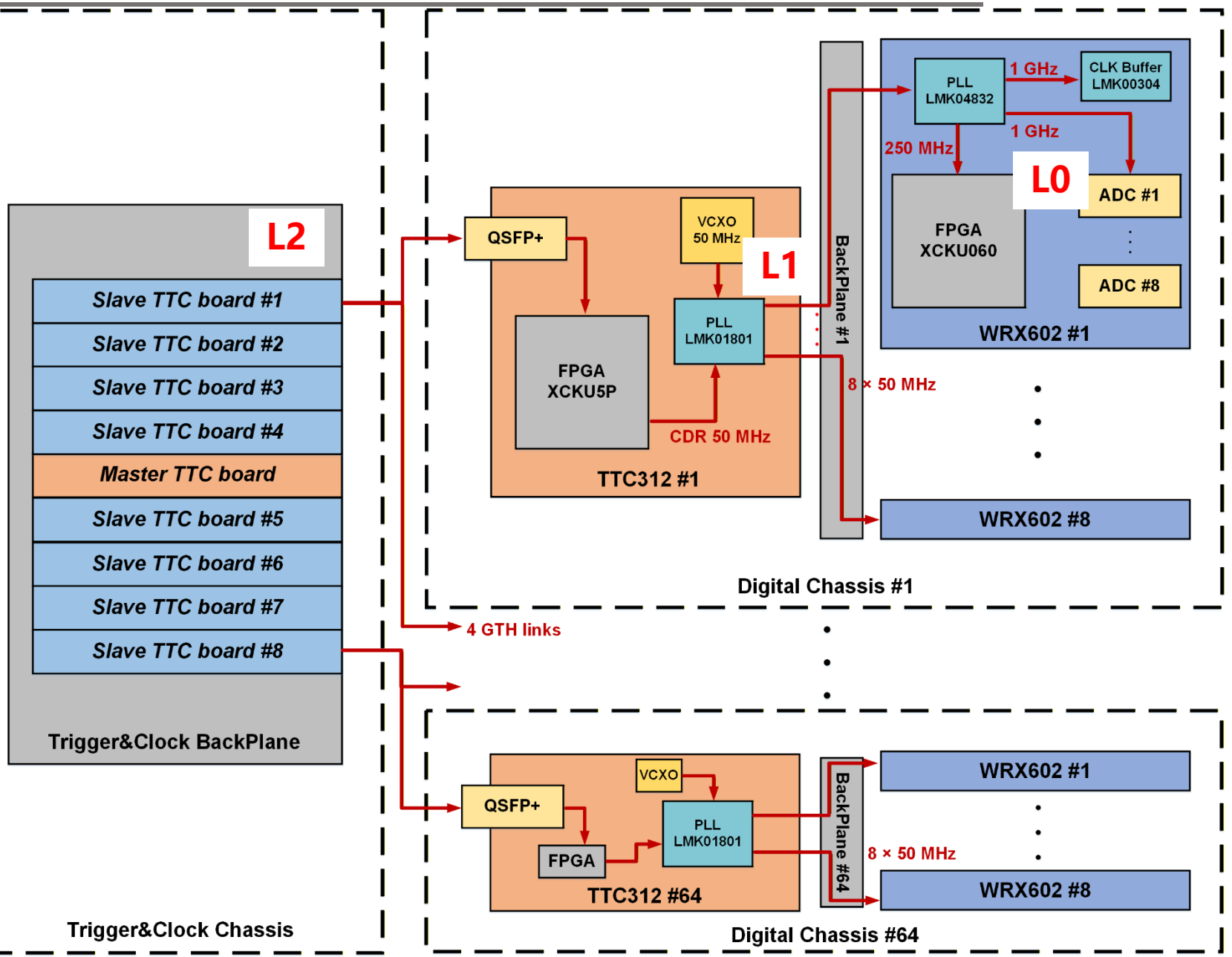

Xiaomi MIMO

Hardware design

- Tsinghua DAQ system
  - Level 2: Chassis
  - Level 1: Board
  - Level 0: Channel

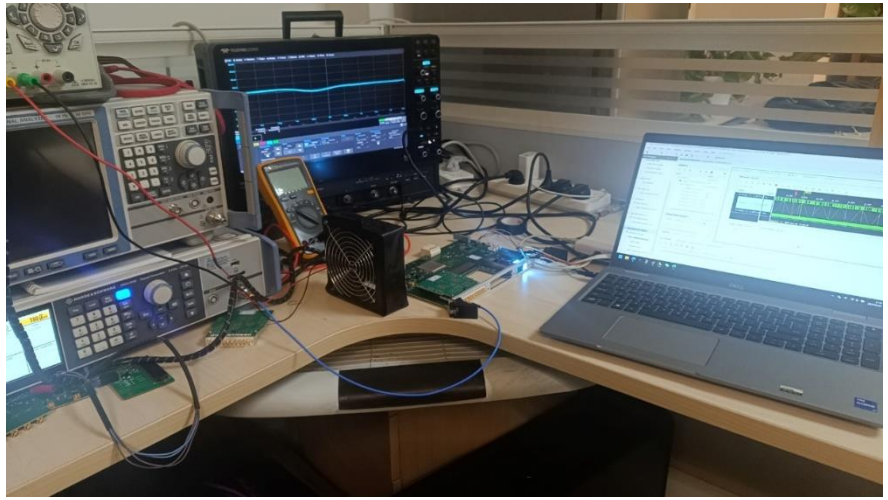






Performance test

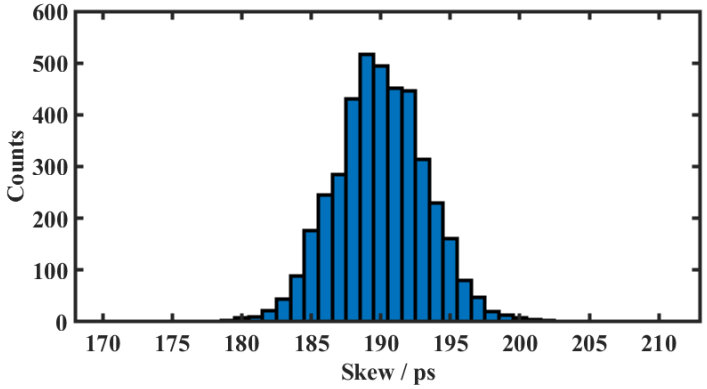
- ADC
  - According to the IEEE-1241 standard, ADC is used to collect the full range 10 MHz sine wave generated by SMA100A
  - $ENOB_{AD9695}$(1 GSPS/14-bit) ~ 10.5 bit

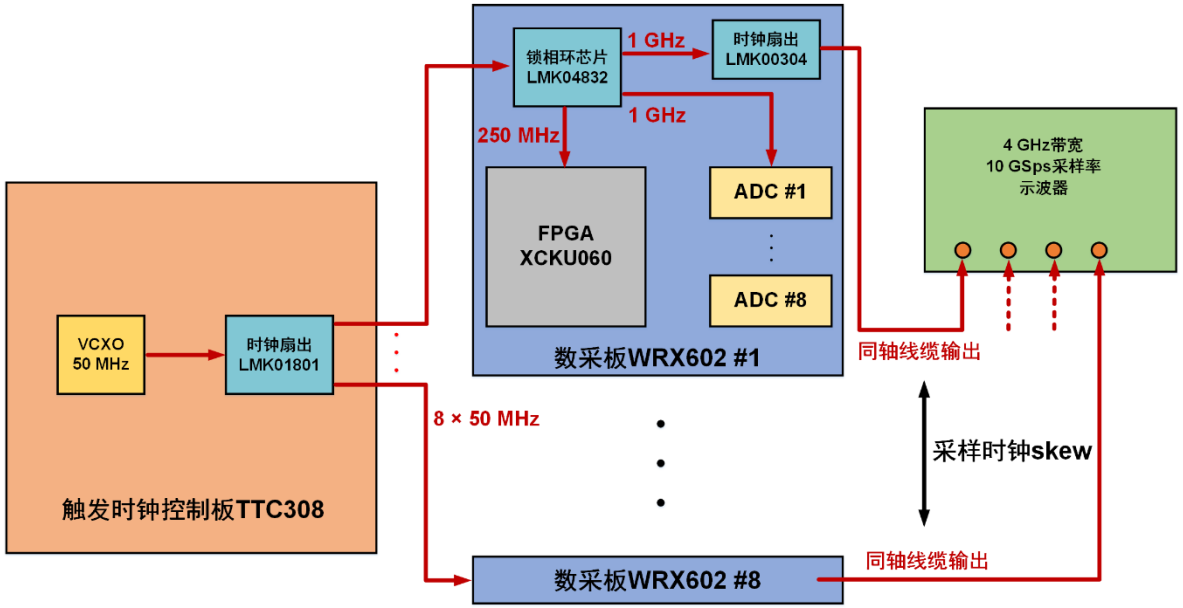


	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
WRX602#1	10.5724	10.5150	10.5365	10.4968	10.4885	10.5667	10.5467	10.4730
WRX602#2	10.5956	10.5556	10.5151	10.4918	10.5574	10.5392	10.4966	10.4922
WRX602#3	10.5681	10.4941	10.5109	10.4718	10.6378	10.5842	10.5868	10.5541
WRX602#4	10.5557	10.5512	10.5154	10.5512	10.4739	10.4873	10.4858	10.5508
WRX602#5	10.4751	10.5206	10.4660	10.5443	10.4662	10.4345	10.5172	10.5394
WRX602#6	10.4696	10.4702	10.5253	10.4762	10.5210	10.4832	10.5830	10.5232
WRX602#7	10.4866	10.5358	10.5328	10.5102	10.5288	10.4852	10.5684	10.4952
WRX602#8	10.4927	10.5114	10.4695	10.5284	10.5026	10.5441	10.5985	10.5038

Performance test

- Time sync
  - Peak position value: 190 ps, can be deducted through calibration
  - Standard deviation:<3 ps, for a physical analysis of a 1 GS/s system, the maximum error that may be introduced is six times the standard deviation of 18 ps

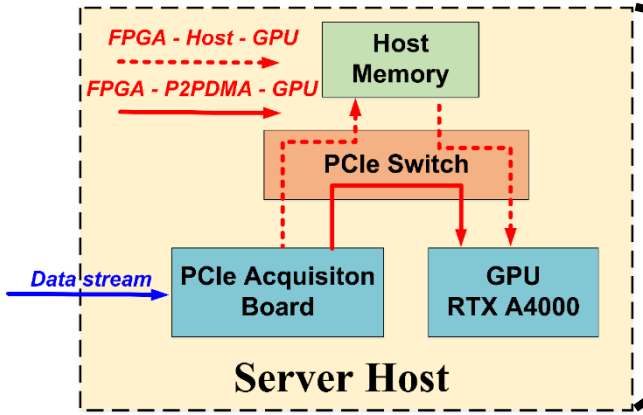


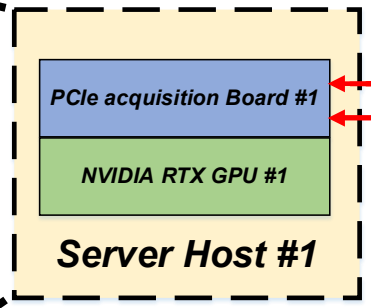


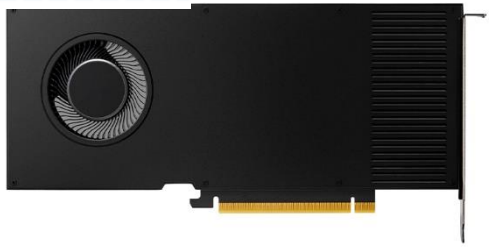
Conclusion

- **A New DAQ System with 64 channels 1 GSps/14-bit ADCs for JNE has been developed**
- **The data bandwidth of PCIe is up to 100 Gbps**
- **The maximum of clock skew between different channels is 20 ps**

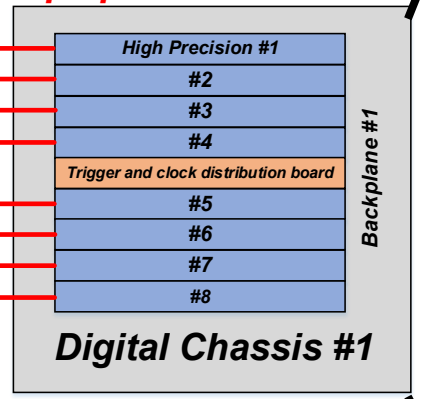
Conclusion

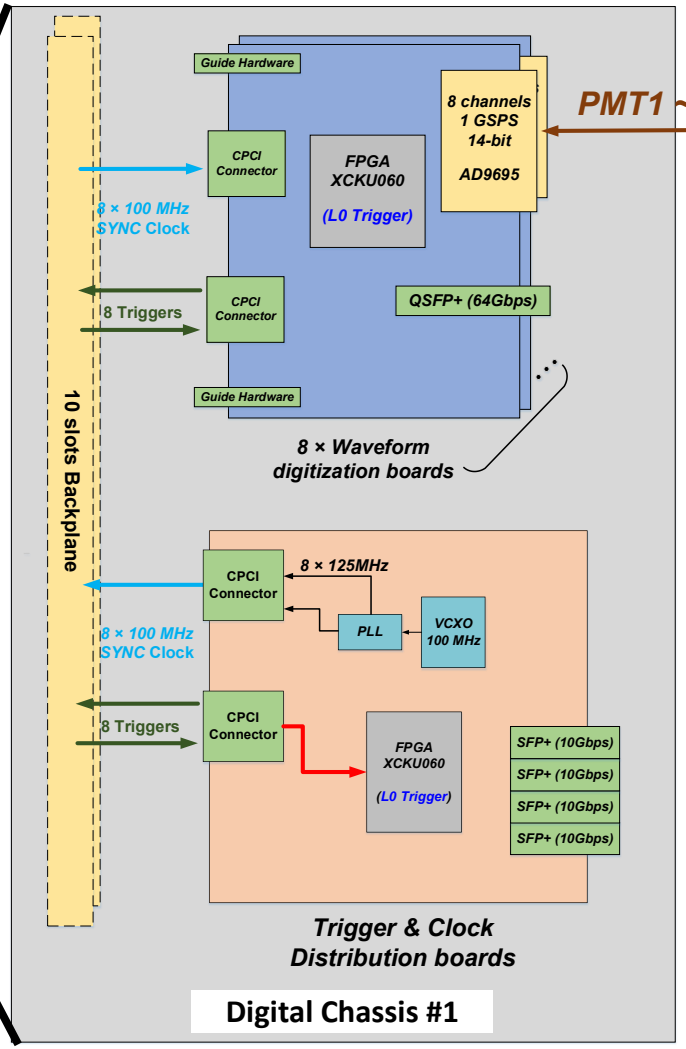






16 Gbps per channel

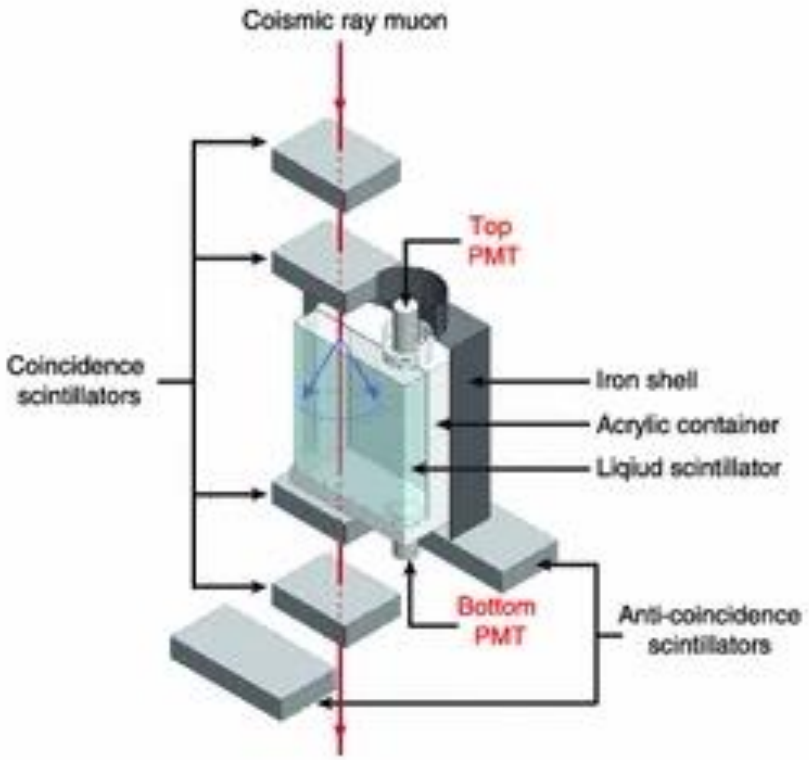




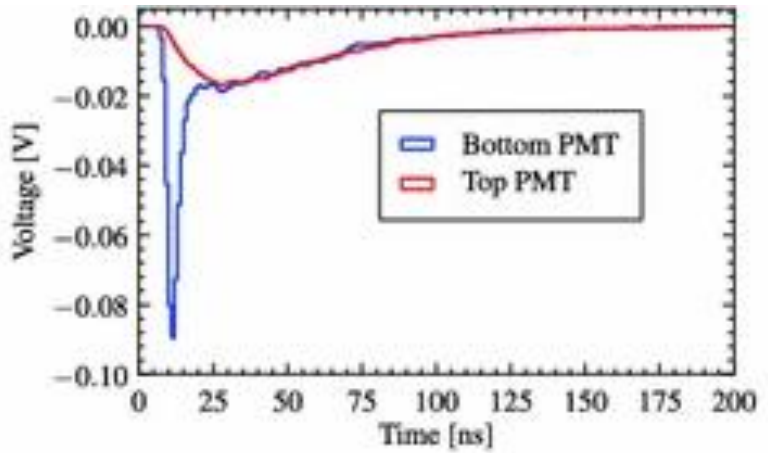
Thanks!

Email : hy-yang22@mails.Tsinghua.edu.cn

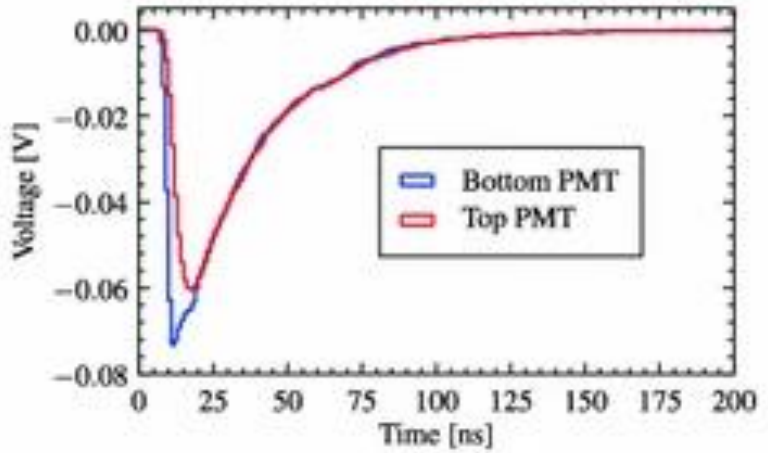
Backup



(a) The structure of the apparatus for light yield and time profile measurement.



(b) Candidate A output waveforms



(c) Candidate B output waveforms

https://doi.org/10.1007/978-981-13-1316-5_32